



Status of the SiWECal TB preparation

Héctor García Cabrera

CIEMAT, Madrid

27 March, 2020



GOBIERNO
DE ESPAÑA

MINISTERIO
DE ECONOMÍA
Y COMPETITIVIDAD

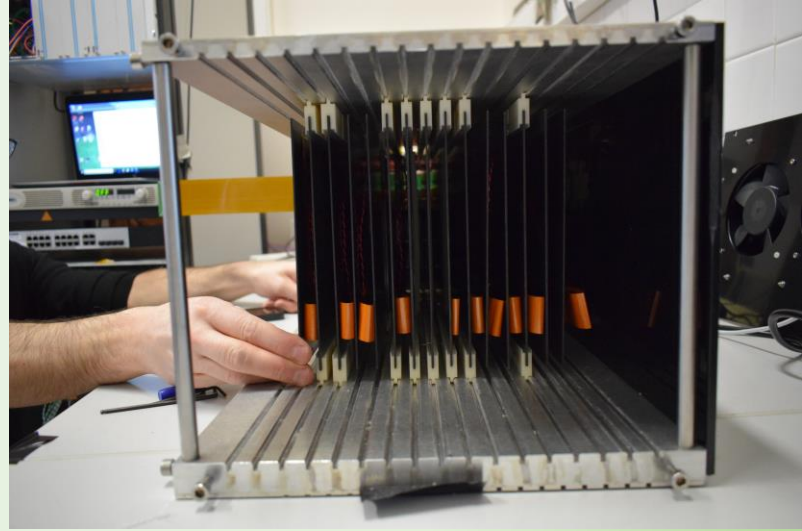
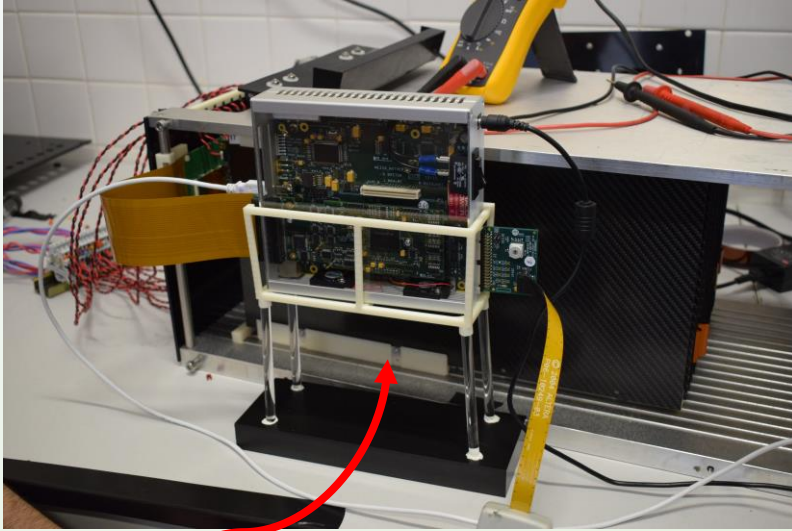
Ciemat

Centro de Investigaciones
Energéticas, Medioambientales
y Tecnológicas

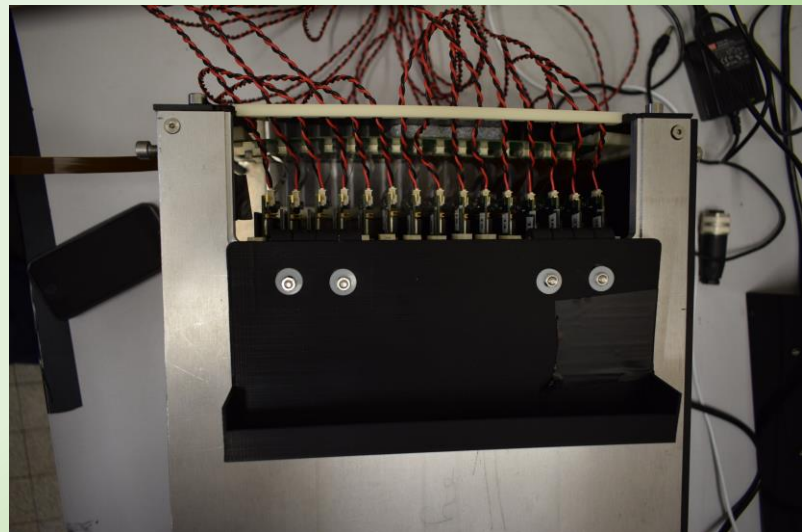


SiW-ECal prototype

A total of 15 layers were installed inside the prototype's box without the absorber (Tungsten) for commissioning.



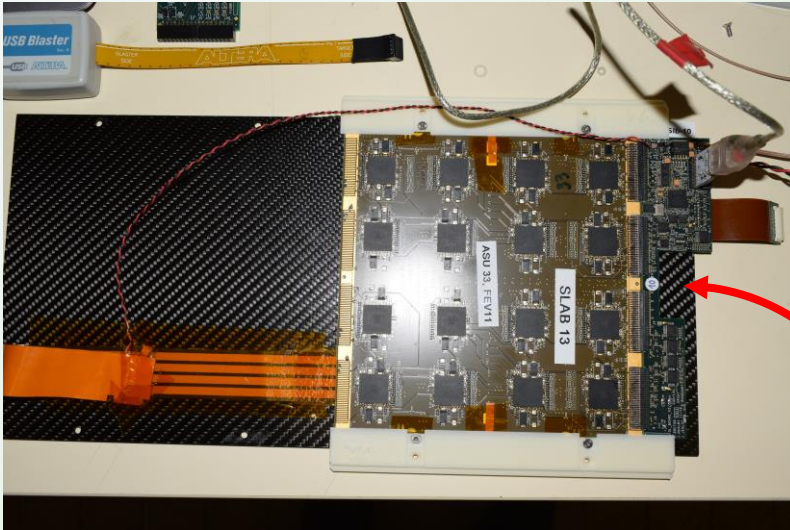
Control and DAQ card for all slabs



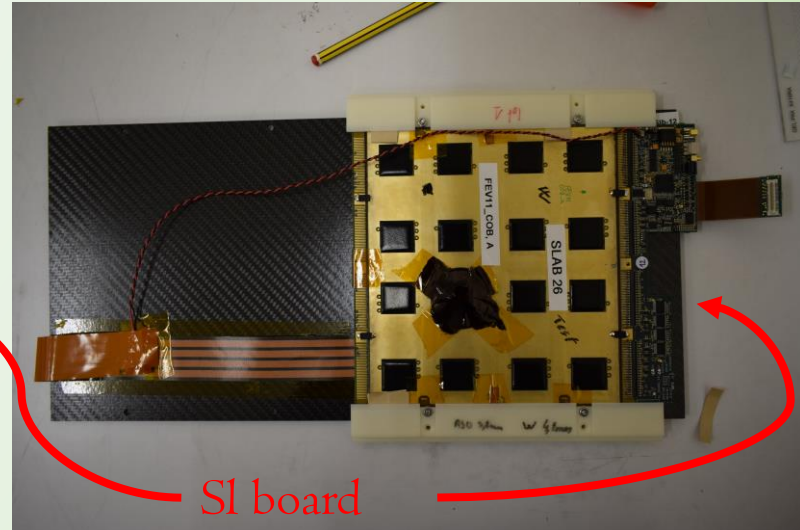
SiW-ECal prototype

Two types of slabs were prepared for the TB:

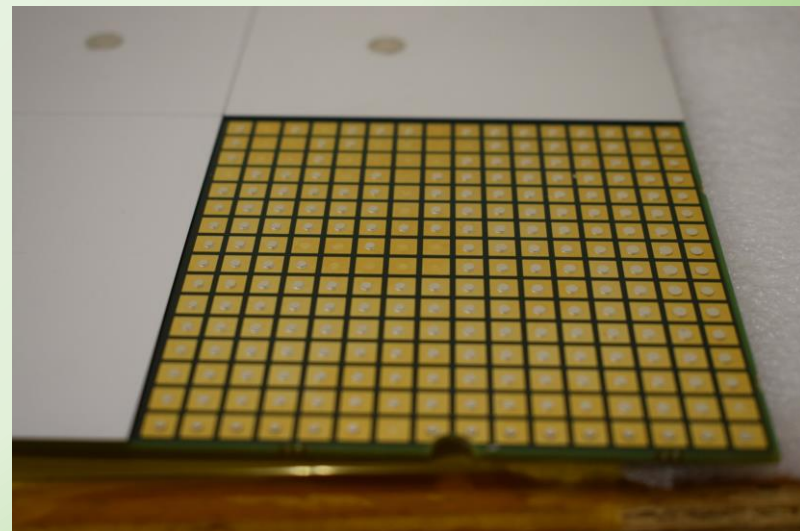
FEV



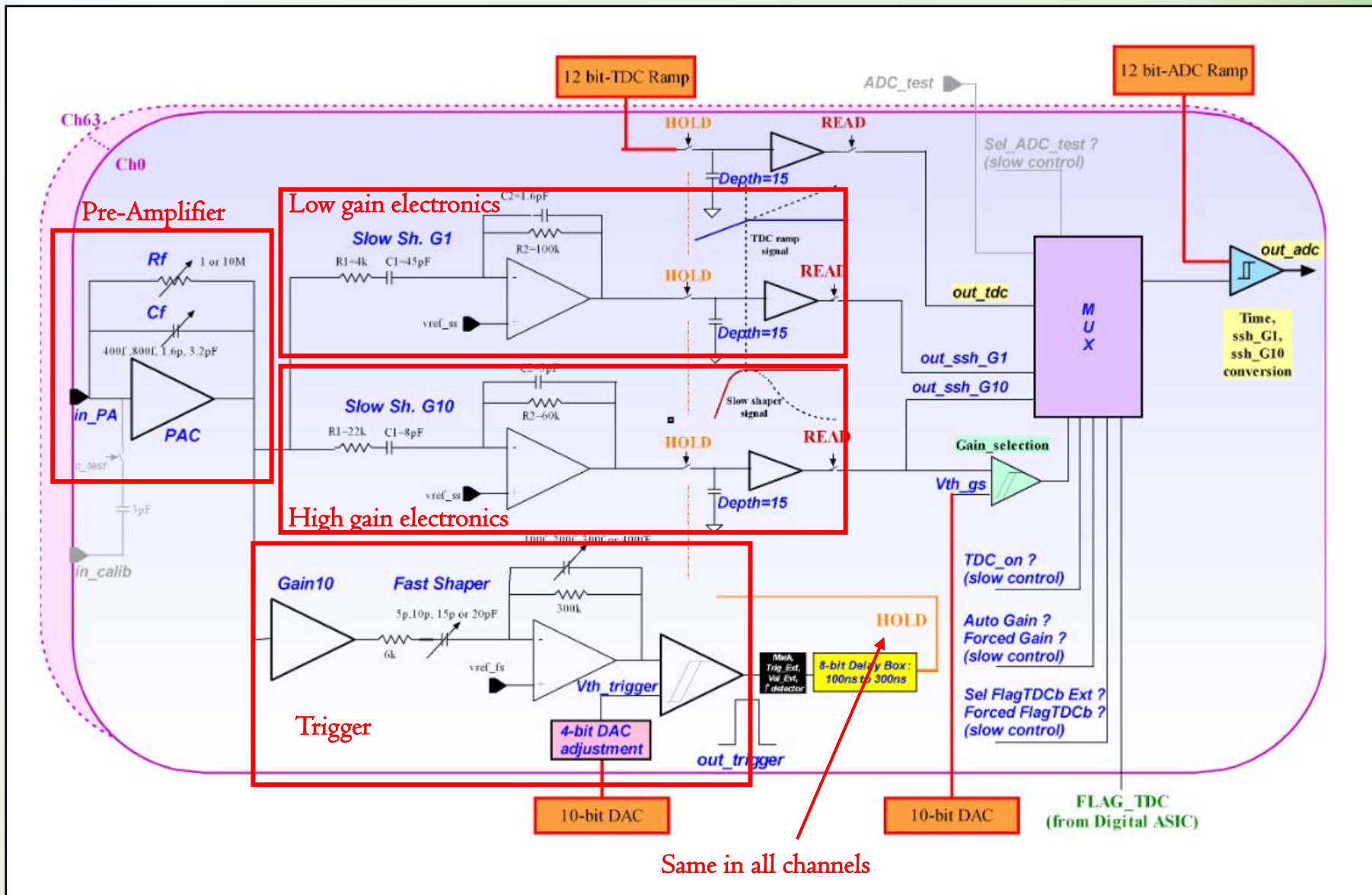
COB



Each slab has 4 silicon wafers with 4 chips per wafer making a total of 16 chips in a slab. A chip controls 64 PIN diode channels. For each channel there are 15 memory cells.

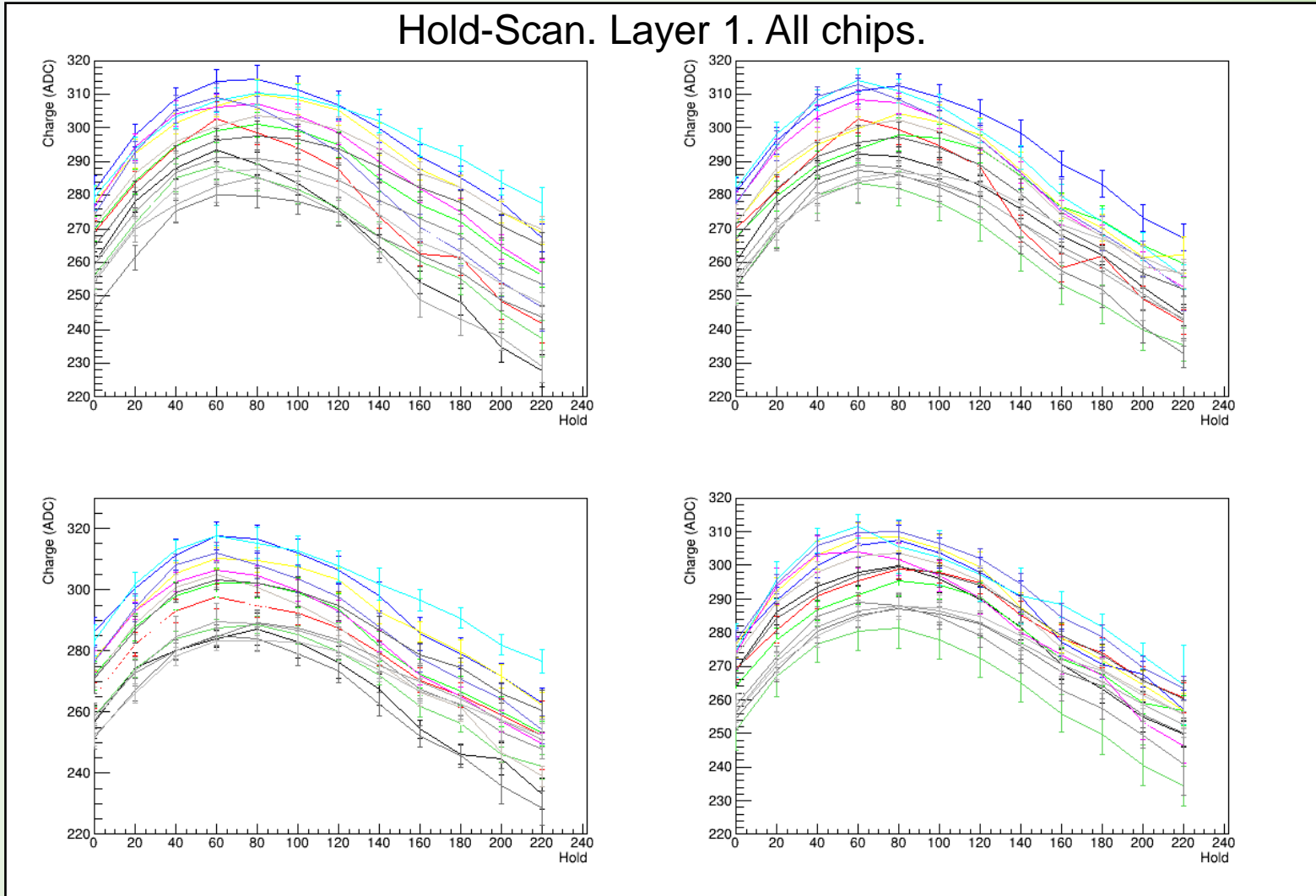


SKIROC: Silicon pin Kalorimeter Integrated ReadOut Chip



SiW-ECal. Hold-Scan

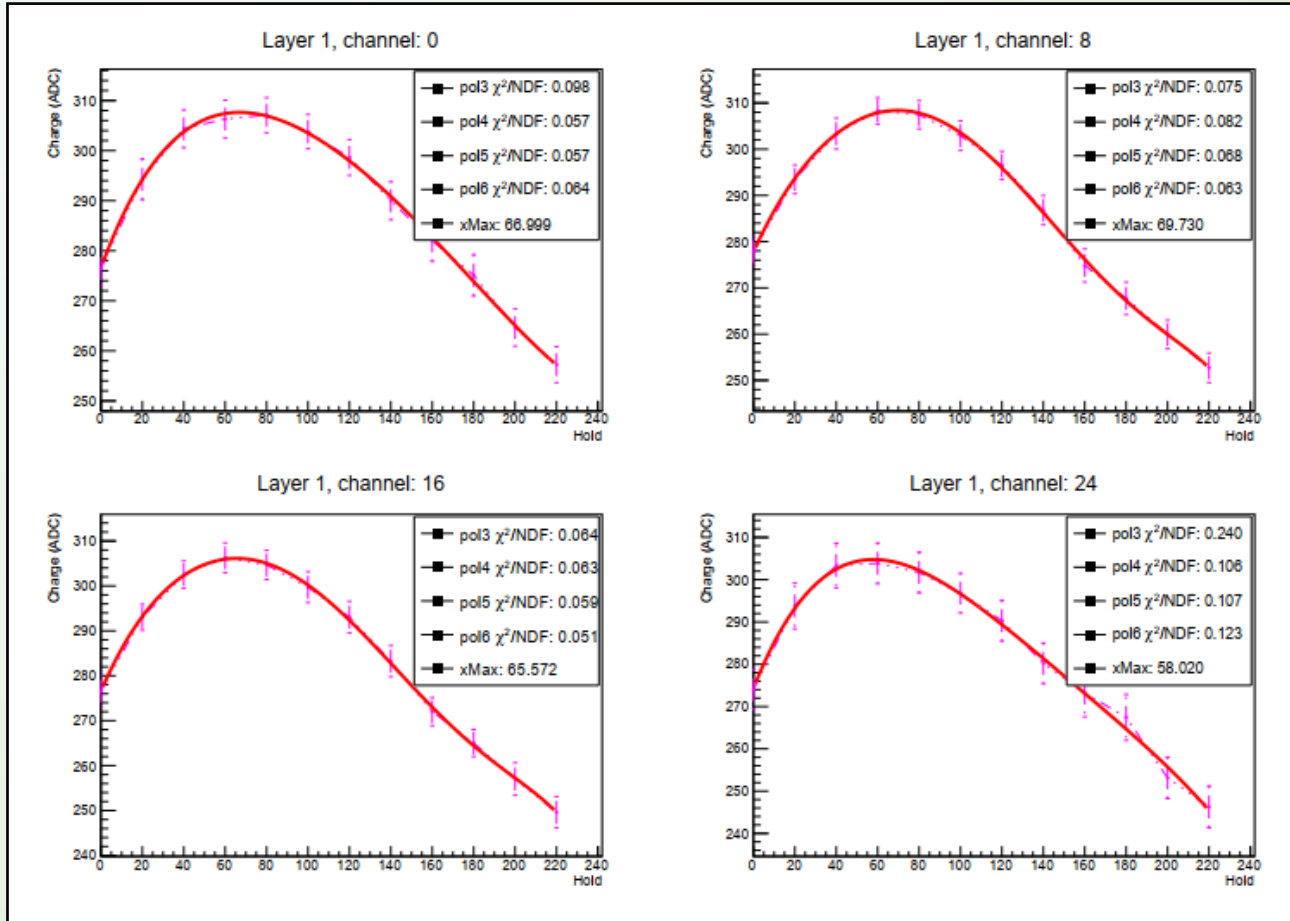
For each chip an optimal value of the hold needs to be found. To do that a small charge (1 MIP approx.) is injected for different values of the hold.



SiW-ECal. Hold-Scan fits

The hold scan is then fitted to a polynomial function to find the maximum and the selected optimal hold value is the mean for all channels.

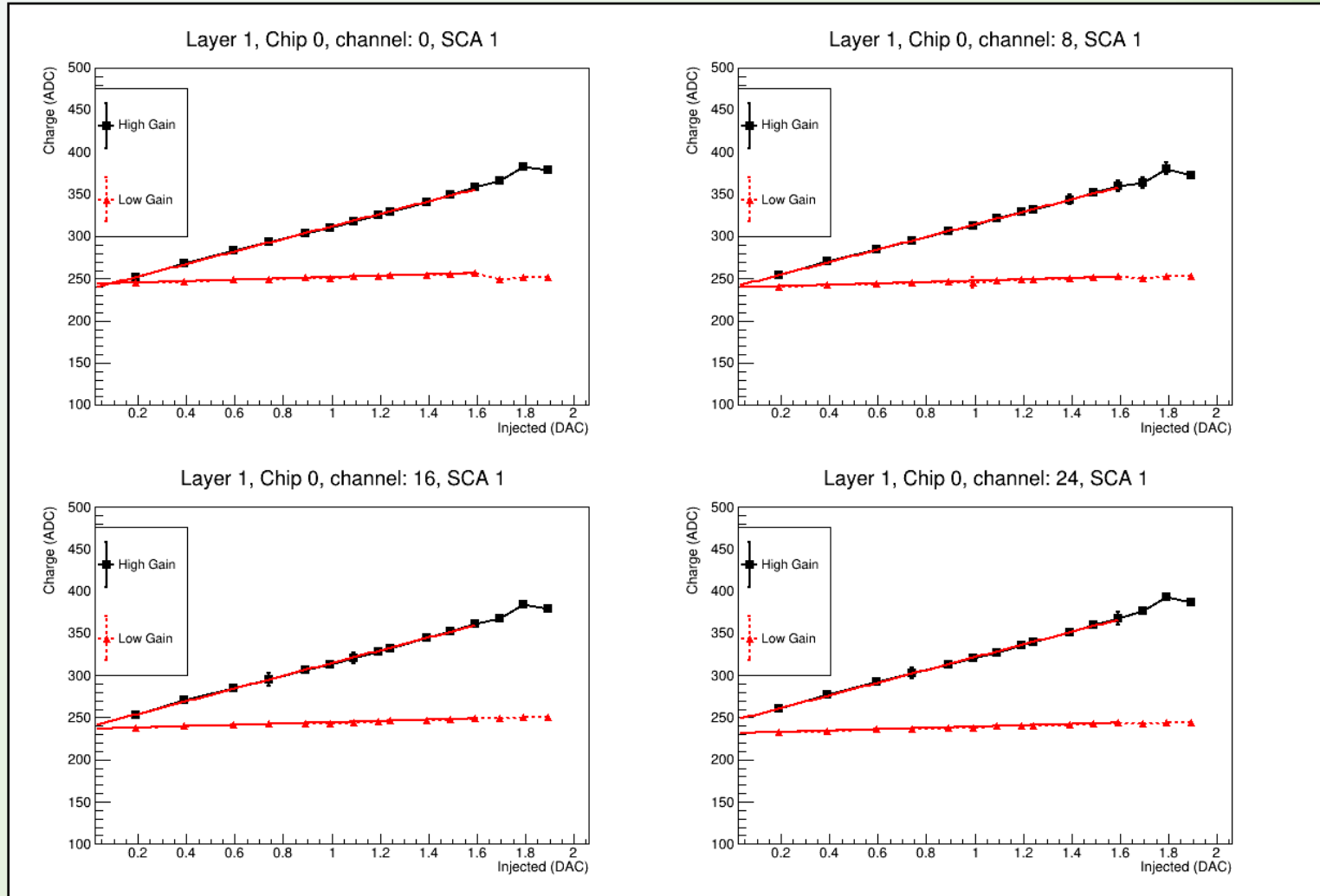
Output File



```
#hold scan results: 20200226_dac1.15V_chn0to3
#layer chip hold error fitfunc
0 0 74.8123 1.59259 pol6 pol6 pol4 pol5
0 1 72.0559 4.10285 pol3 pol5 pol5 pol4
0 2 81.5356 7.04917 pol4 pol3 pol6 pol4
0 3 94.0402 3.99469 pol4 pol4 pol6 pol4
0 4 140.216 89.7758 pol3 pol6 pol5 pol6
0 5 62.1894 1.8918 pol3 pol5 pol3 pol3
0 6 95.1555 33.5164 pol5 pol6 pol5 pol5
0 7 89.6917 59.6565 pol6 pol6 pol3 pol3
0 8 62.11 2.26285 pol3 pol6 pol6 pol5
0 9 73.5652 1.5959 pol4 pol5 pol6 pol6
0 10 78.8351 8.41269 pol5 pol3 pol5 pol5
0 11 85.5032 7.4936 pol6 pol3 pol5
0 12 52.2774 51.6465 pol3 pol3 pol6 pol4
0 13 89.2618 51.5803 pol6 pol5 pol6 pol3
0 14 53.2831 30.9809 pol3 pol4 pol6 pol3
0 15 84.4835 6.96193 pol3 pol5 pol5
1 0 71.5066 7.61075 pol5 pol4 pol6 pol6
1 1 72.758 7.48302 pol5 pol5 pol4 pol6
1 2 80.0483 5.66974 pol5 pol6 pol6 pol4
1 3 74.8822 3.10136 pol6 pol3 pol5 pol6
1 4 78.1894 5.80729 pol6 pol4 pol5 pol6
1 5 65.0804 4.34149 pol5 pol6 pol6 pol4
1 6 67.5325 8.91708 pol4 pol5 pol6 pol6
1 7 67.4142 3.37813 pol6 pol4 pol3 pol4
1 8 64.6871 3.79291 pol5 pol6 pol5 pol4
1 9 76.9834 7.14202 pol6 pol5 pol6 pol4
1 10 73.5779 8.15409 pol3 pol6 pol4 pol6
1 11 76.925 5.07873 pol4 pol6 pol5 pol6
1 12 73.0187 4.45532 pol6 pol5 pol5 pol3
1 13 73.8021 8.57451 pol6 pol6 pol6 pol5
1 14 77.2308 3.1157 pol6 pol6 pol5 pol5
1 15 81.8692 4.53601 pol3 pol3 pol3 pol6
2 0 76.2857 4.46375 pol3 pol3 pol5 pol3
2 1 77.6629 2.80281 pol6 pol3 pol4 pol6
2 2 77.1537 2.04207 pol3 pol6 pol5 pol6
2 3 78.6167 2.1476 pol5 pol4 pol5 pol4
2 4 69.2506 1.52198 pol3 pol5 pol5 pol5
2 5 74.0519 5.79192 pol3 pol3 pol6 pol3
```

SiW-ECal. Pedestal search

Once the value of the hold is fixed, several different charges are injected. The pedestal is found with the fit to a straight line at zero injected charged. Due to different paths in the electronics there is a pedestal for high and low gains in each channel and memory cell.



Summary

The output files from the hold-scans and the pedestal search are needed for the event building procedure.

However, these analysis were made with a preliminary test injecting charge in only 4 channels.

Work on hold due to current “situation”:

- Data taking for all channels with the final setup.
- Event building and reconstruction of events.
- Development of a fast and simple event display for debugging.

Back-up