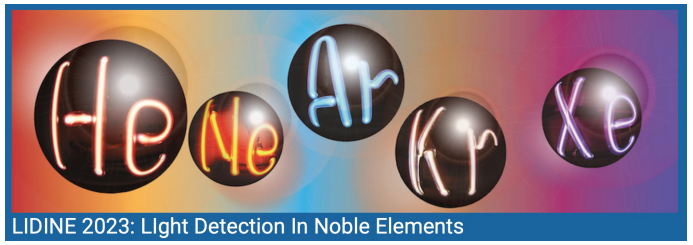

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U.S. DEPARTMENT OF ENERGY

Front-end CMOS Application Specific Integrated Circuits (ASICs) for Light and Charge Readout

Prashansa Mukim, Grzegorz Deptuch, Gabriella Carini, Hucheng Cheng, Shanshan Gao, Dominik Gorni, Jay Hyun Jo, Lingyun Ke, Steven Kettel, Soumyajit Mandal, Xin Qian, Sergio Rescia, Chao Zhang

September 22, 2023

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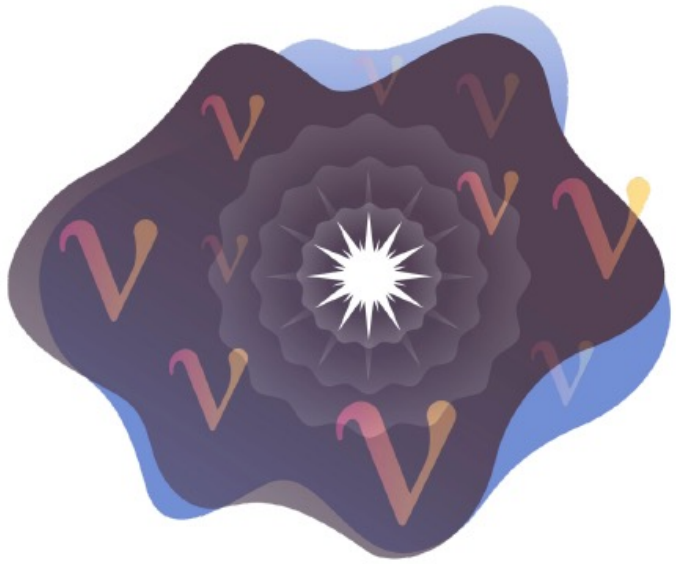
Designed for DUNE : Deep Underground Neutrino Experiment

Primary science goals

Study neutrino/antineutrino oscillations



Detect neutrinos emerging from exploding stars

Search for signs of proton decay

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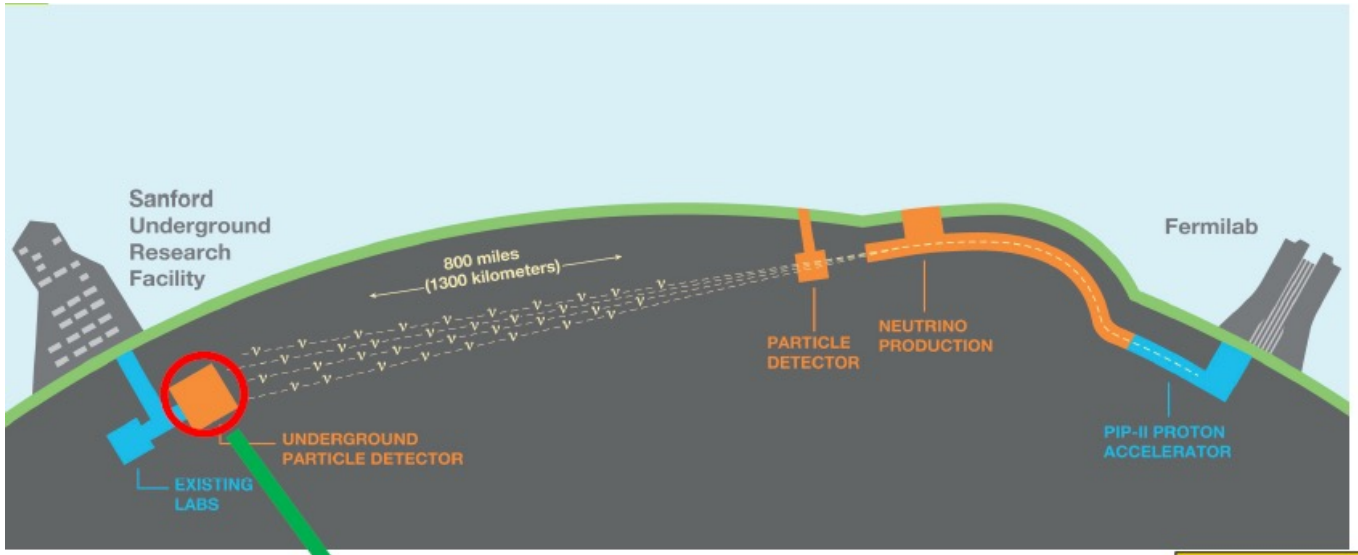
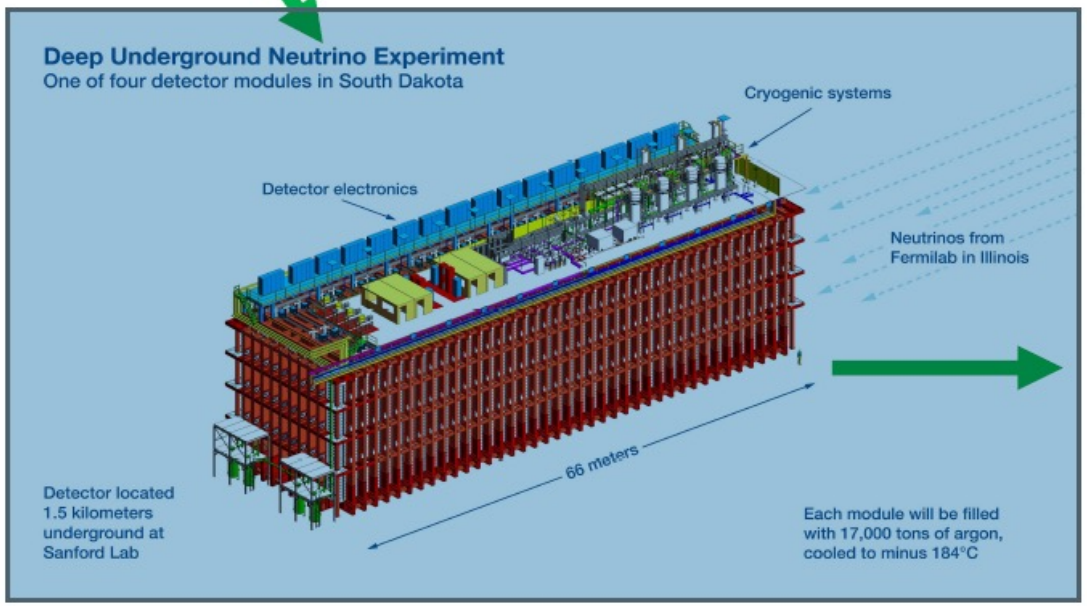
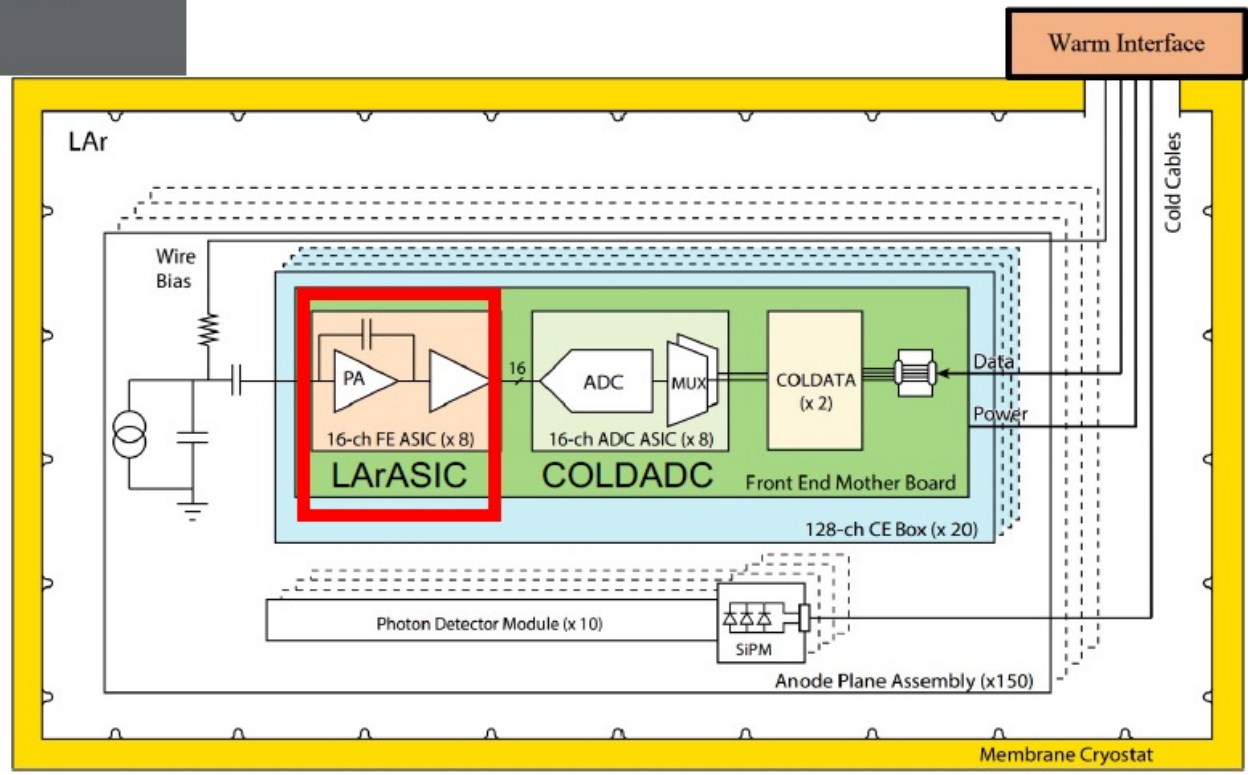
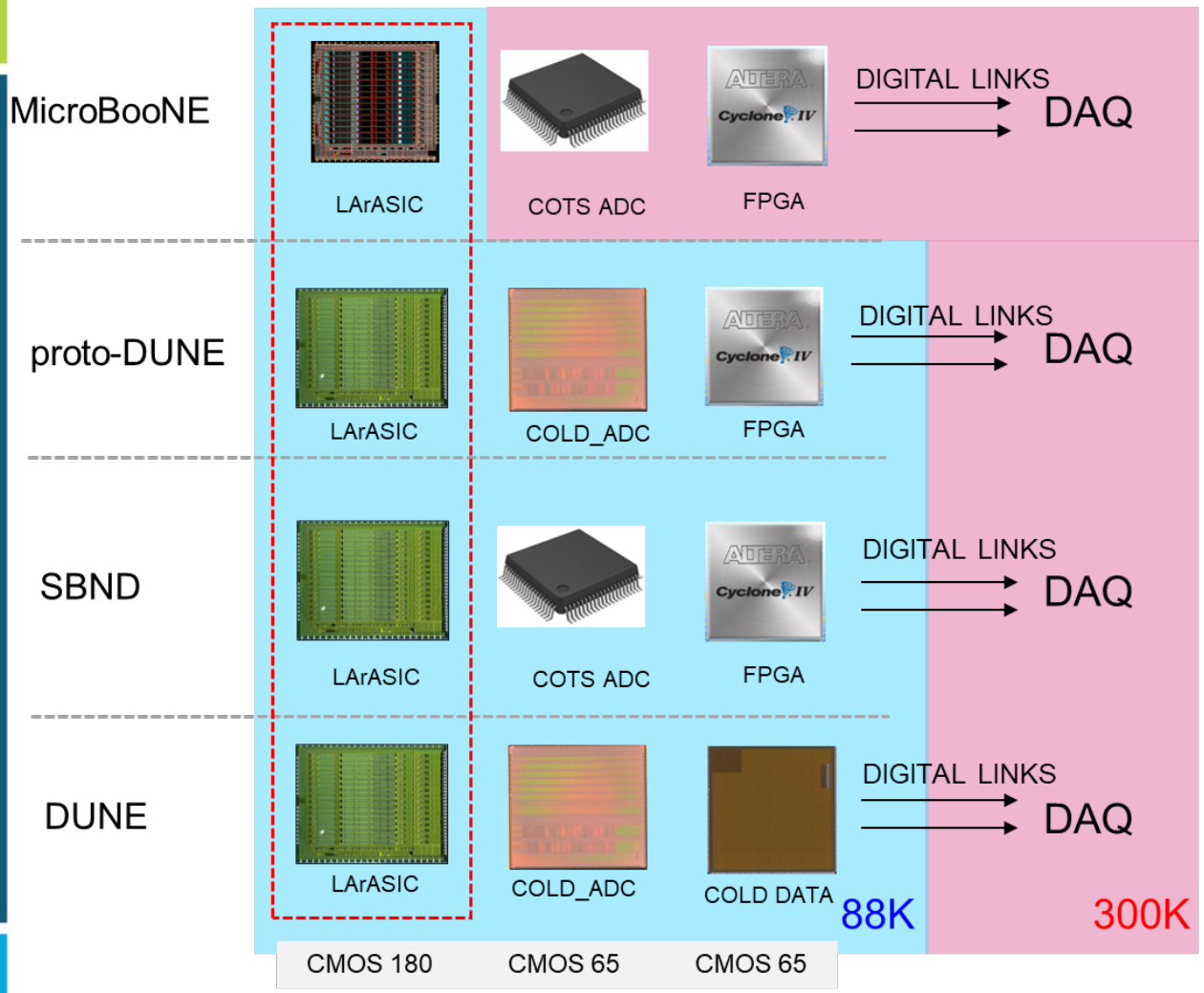


- Currently deployed for readout at the Single-Phase (SP) Liquid Argon (LAr) Time-Projection Chamber (TPC) for Far Detector (FD)
- 3-chip solution for energy measurement, includes: charge amplification, shaping, digitization and serial readout
- Front-end (FE) electronics close to the detector enables readout at low-noise
- Need to ensure FE operates reliably at 87 K





Status of ASICs in DUNE



3 ASICs vs. 1 ASIC solution:

- Initially two readout options were proposed:
  - 3 ASICs vs. 1 ASIC
    (idea of building 1 ASIC, combining FE/ADC/transmission brought in 2016 and included as parallel path of development)
- Evolutionary development MiCroBooNE → DUNE led to the 3 ASIC solution that:
  - Helped perfect the FE (through multiple iterations)
  - Allowed debugging (procedure for ADC calibration)
  - Allowed optimization

About a decade of development

LArASIC – status

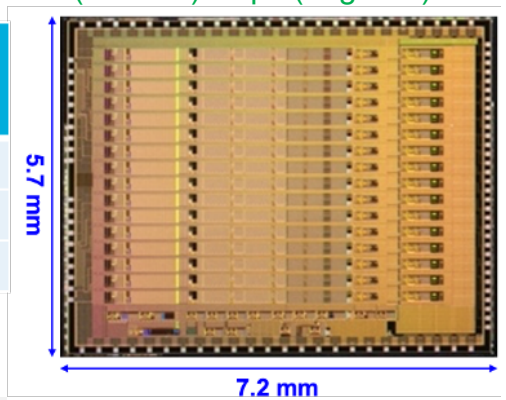
LArASIC MPW met all the DUNE requirements → fabricated ~1800 P5 and 1800 P5B (180 nm) chips (eng. run) for ProtoDUNE II

LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5	RT	49	49	100 %
P5B	**RT**	**1642**	**1635***	**~99.57 %**
P5B	**LNT**	**317**	**317**	**100 %**

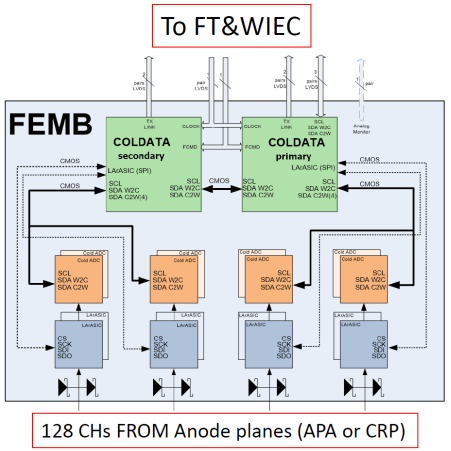
P5B has improved input ESD protection compared to P5

*Only 1 out of 16 channels in each of the two chips are non-functional

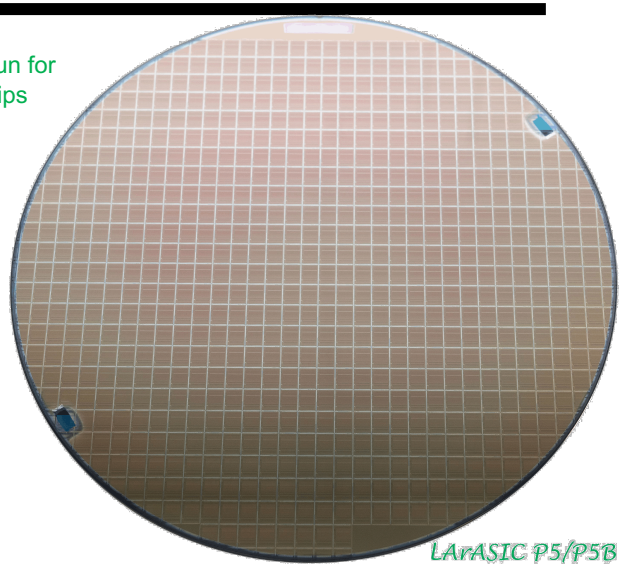
>6 months ago, now more statistics is available



LArASIC performance with differential interface



250 wafers LArASIC production run for DUNE 75k P5 and 75k P5B chips



8" wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

Design currently being translated to 65 nm CMOS

already 24 FEMBs arrived at CERN for ProtoDUNE-II installation

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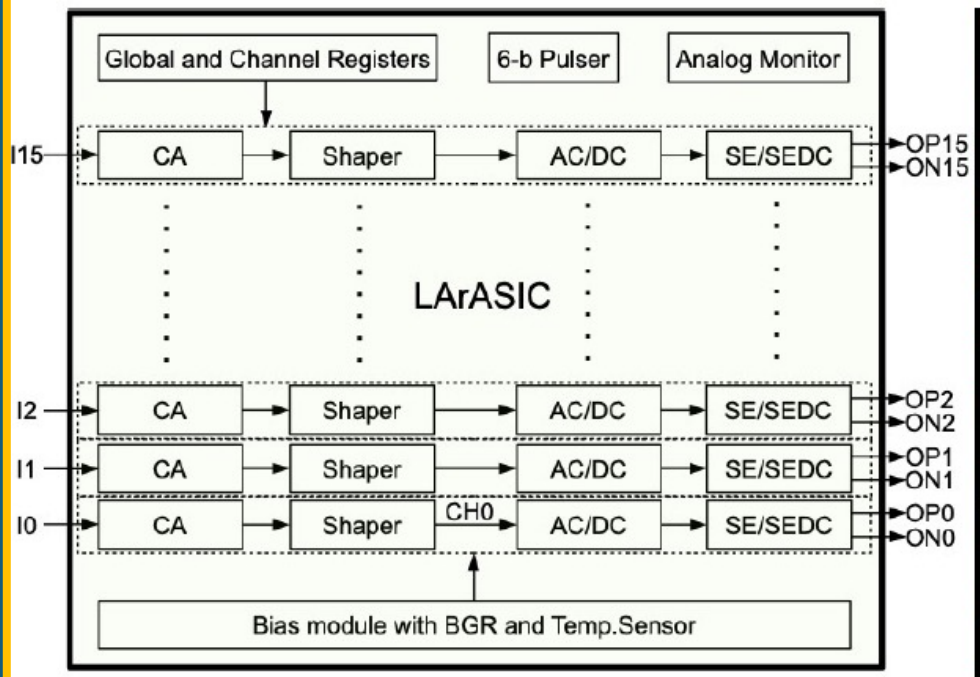
LArASIC – block diagram and specifications

LArASIC (P5B)



Technology	180 nm CMOS – 1-poly, 6-metal, MiM cap, sil blk resistors			
Supply Voltage	1.8 V			
Temperature Range	77 – 300 K (-196 – 27 °C) optimized for 87k (-186 °C)			
Number of Channels	16			
Max Single-Ended Output Swing	1.4 V peak to peak (0.2 – 1.6 V)			
Gain Selection (mV/fC)	4.7	7.8	14	25
Full-Scale Input Charge (fC)	300	180	100	56
Baseline selection	200 mV (collection mode)		900 mV (induction mode)	
Charge Preamplifier Polarity	Negative (collection mode)		Bipolar (induction mode)	
Adaptive-Reset Current Selection (nA)	0.1	0.5	1	5
Shaper Peaking Time Selection (µs)	0.5	1	2	3
Output Coupling	AC (100 µs HPF time-constant)		DC	
Output Selection	Shaper	SE buffer	SEDC buffer	
Total Channel Settings	1024			
Integrated Test Capacitor	200 fF			
Temperature Sensor	0.8728 V @ 25°C + 2.868 mV/°C			
Integrated Pulse Generator	6-bit DAC based			
Configuration Control	SPI interface with 144 register bits			

New design
(yet to be fabricated)

65 nm CMOS: 1-poly, 9-metal
✓
✓
✓
✓
✓
✓
✓
✓
✓
✓
✓
I²C interface

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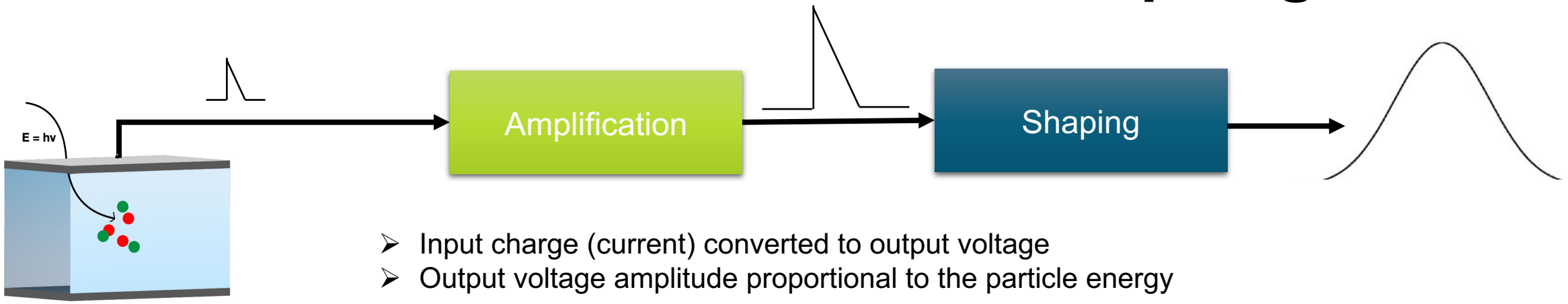
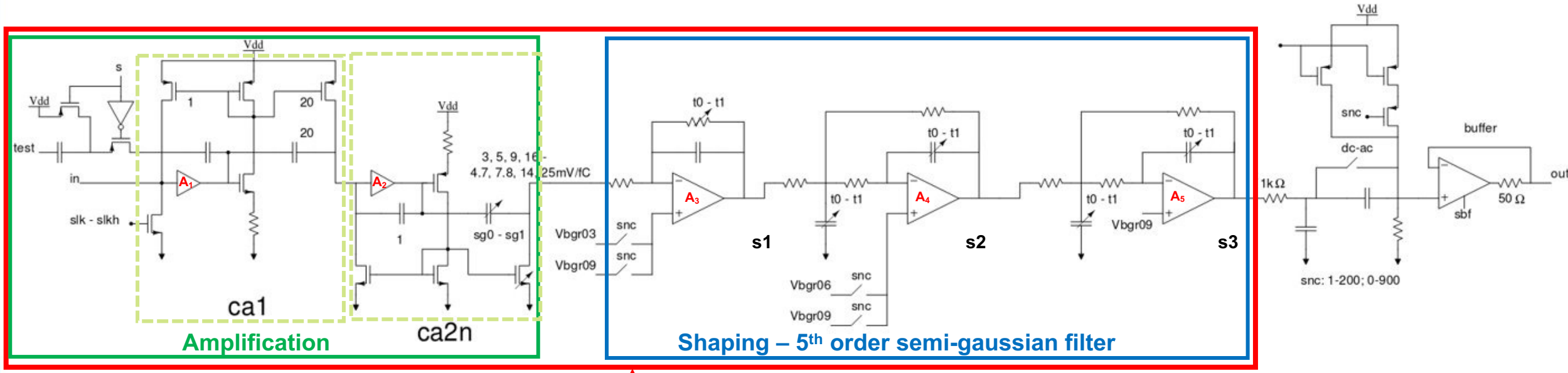
LArASIC architecture / circuit topologies



- Input charge (current) converted to output voltage
- Output voltage amplitude proportional to the particle energy



Design in 65 nm completed with 3 mW power consumption

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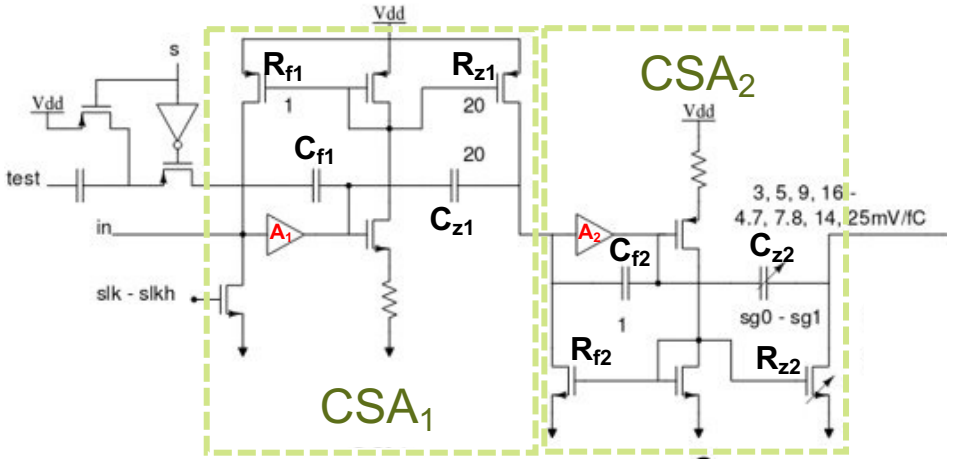
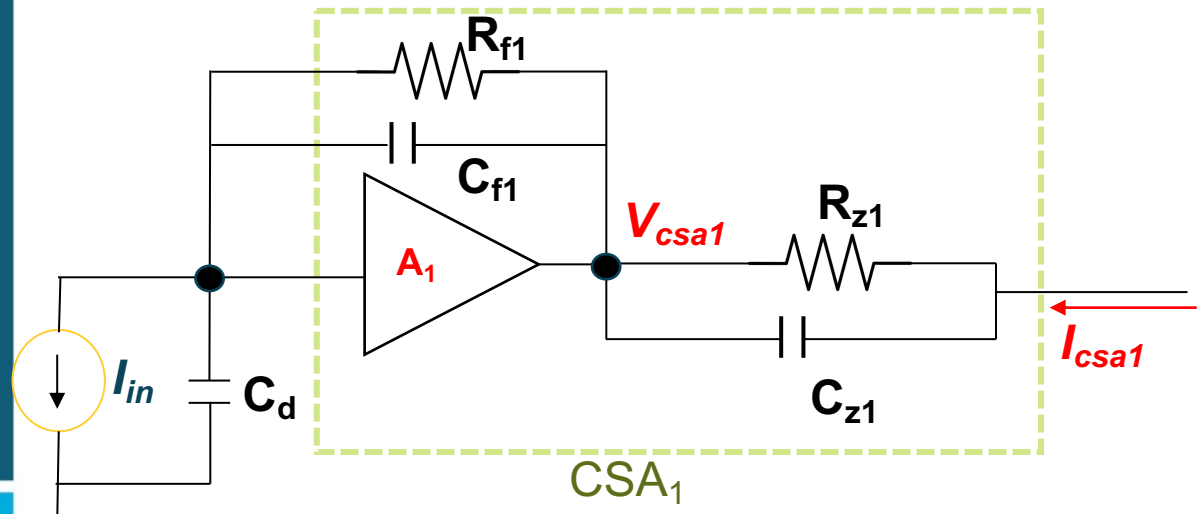
Charge Sensitive Amplifier design





- Charge amplifiers use current-mirror based adaptive continuous reset
- A_1 and A_2: 3-stage amplifiers (> 100 dB gain)
- Pole zero cancellation ($C_fR_f = C_zR_z$) ensures fast I_{csa1} pulse and prevents baseline drift

$$I_{csa1}(s) = \underbrace{I_{in}(s)\frac{R_{f1}}{(1+sC_{f1}R_{f1})}\frac{(1+sC_{z1}R_{z1})}{R_{z1}}}_{V_{csa1}}$$

- $C_{z1} = 20C_{f1}$, $R_{z1} = (1/20)R_{f1}$, charge gain provided by $CSA_1 = 20$
- $C_{z1} = (3 \text{ or } 5 \text{ or } 9 \text{ or } 16)C_{f1}$, $R_{z1} = (1/3 \text{ or } 1/5 \text{ or } 1/9 \text{ or } 1/20)R_{f1}$, charge gain (programmable) provided by $CSA_2 = 3$ or 5 or 9 or 16

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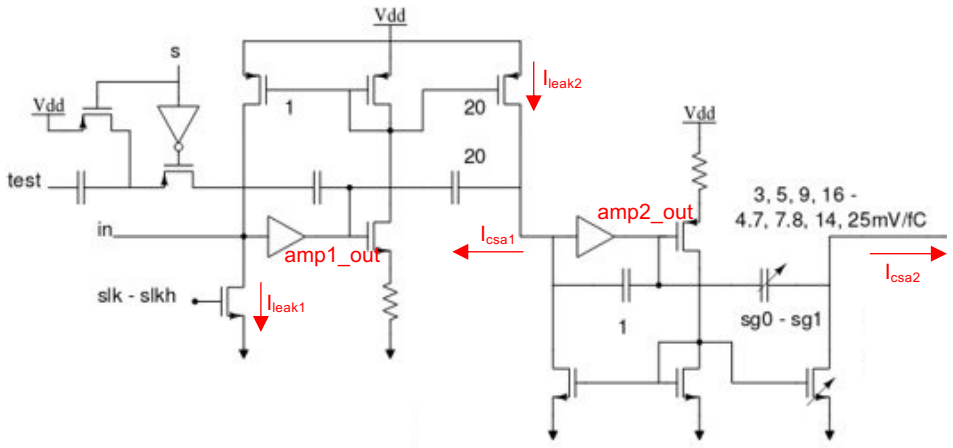
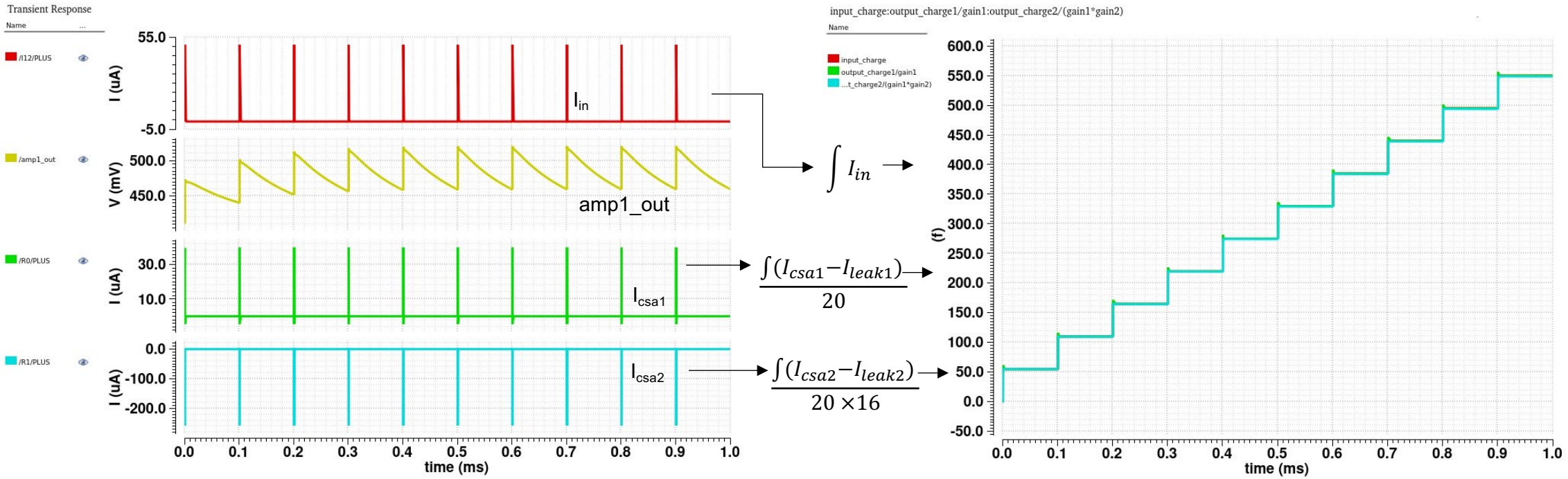
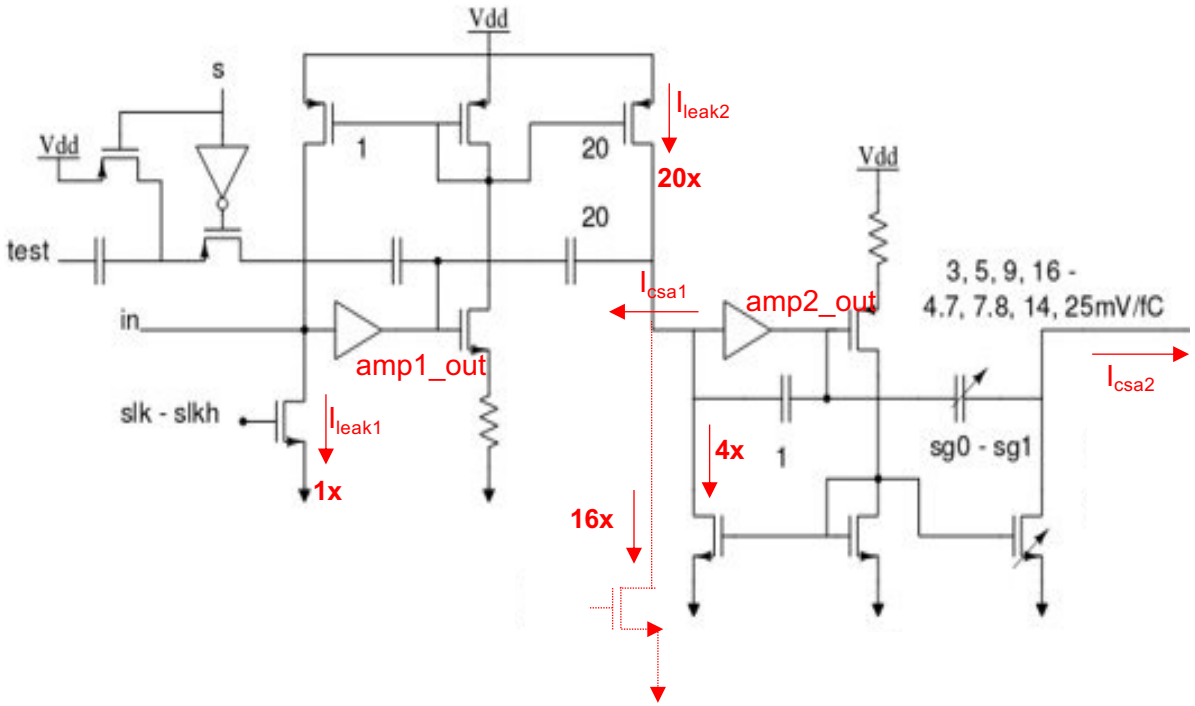
CSA_1 and CSA_2 charge multiplication check





CSA_2 reset (leakage) current subtraction



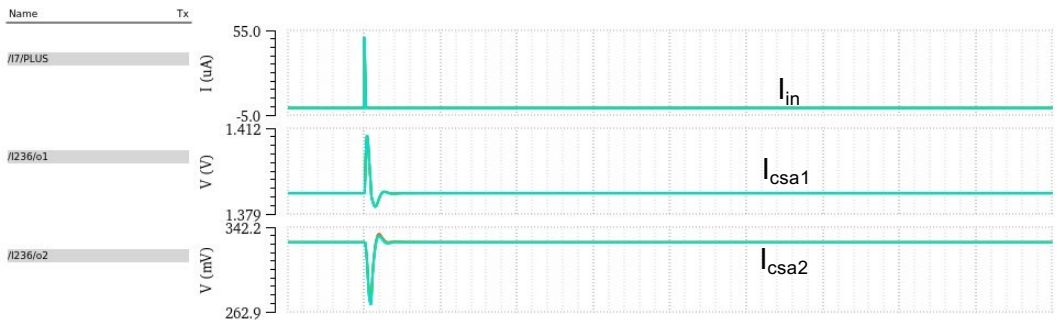
- Reset Quiescent Current (RQI) subtraction for CSA_2 to be implemented in the new design
- Prevents propagation of leakage current and corresponding baseline shift
- To be made programmable independently for each channel

Gain and bandwidth comparisons for amplifiers

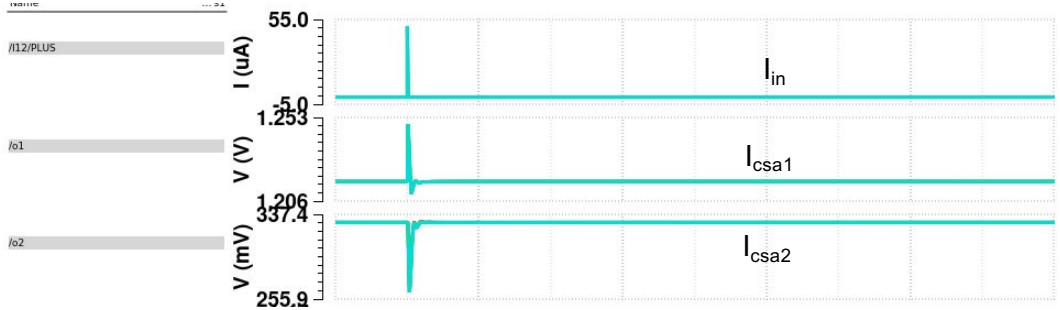
A_1		
	Gain	**Bandwidth**
180 nm	93 dB	4 MHz
65 nm	113 dB	10 MHz

- Higher amplifier gain => more precise current multiplication
- Higher amplifier bandwidth => faster output response

A_2			
	Setting	**Gain**	**Bandwidth**
180 nm	**4.7 mV/fC**	104 dB	42 MHz
	7.8 mV/fC		31 MHz
	14 mV/fC		21 MHz
	25 mV/fC		14 MHz
65 nm	**4.7 mV/fC**	114 dB	56 MHz
	7.8 mV/fC		45 MHz
	14 mV/fC		32 MHz
	25 mV/fC		22 MHz

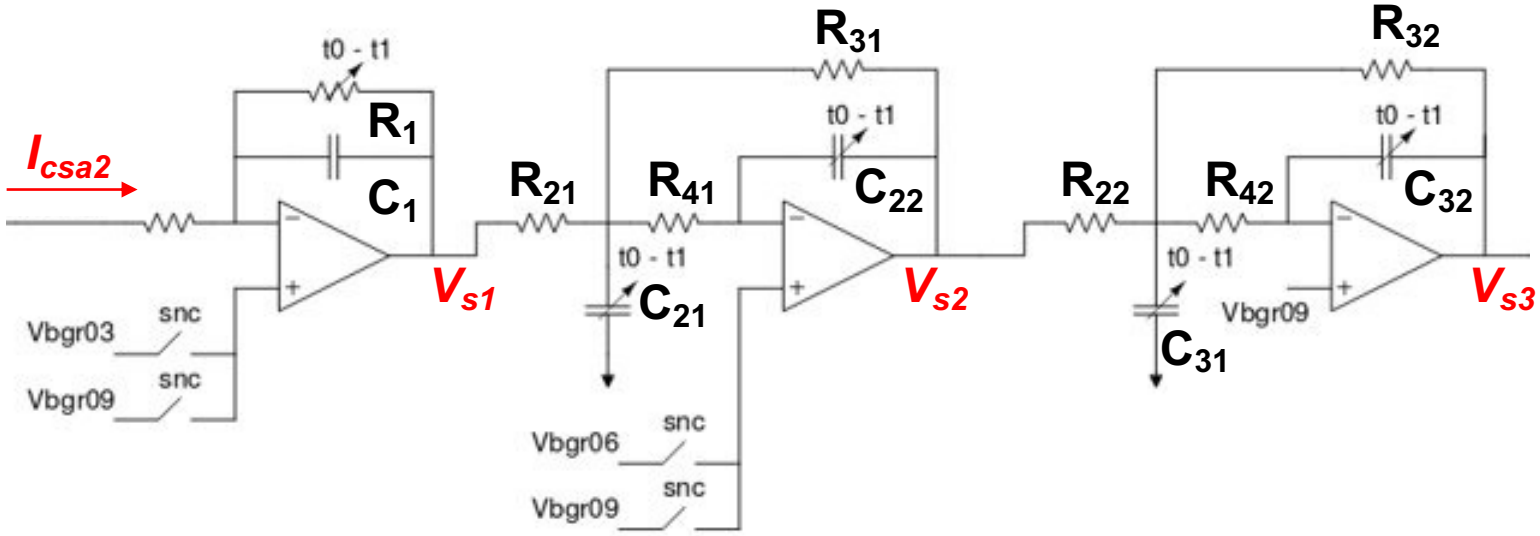


180 nm



65 nm

Shaper design



- Implemented shaper is a 5th order semi-gaussian filter with complex conjugate poles
- V_{csa2} output is a fast pulse, poses stringent requirements on peak capturing circuit (must be fast and accurate)
- Shaper slows down the variations near signal peak
- (Nearly) equal rise and fall times maximize the output signal amplitude for a given pulse duration

$$V_{s1}(s) = I_{csa2}(s)\frac{R_1}{(1+sC_1R_1)}$$

$$V_{s2}(s) = V_{s1}(s)\frac{\frac{1}{R_{21}R_{41}C_{21}C_{31}}}{s^2 + s\left(\frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}}\right) + \frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar……

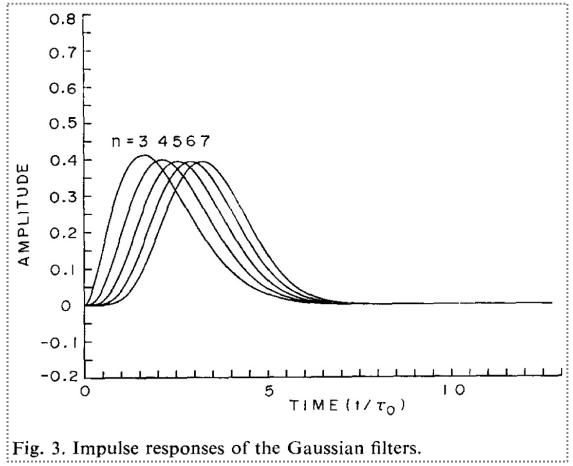


Fig. 3. Impulse responses of the Gaussian filters.

S. Ohkawa, M. Yoshizawa, K. Husimi,
Direct synthesis of the Gaussian filter for nuclear pulse amplifiers.

Noise minimization strategy

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of white noise, 1/f noise and shot noise components)

Input stage transistors for A_1 implemented using thick oxide (2.5 V) devices in 65 nm to limit leakage current and associated shot noise

$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input stage transistor sized to have C_g ~ 40 pF, optimal choice for minimizing noise with C_{det} ~ 150 pF with given power budget

	Minimum allowable transistor length	Input transistor length	Input transistor width
180 nm	180 nm	270 nm	20 mm
65 nm	280 nm	400 nm	24 mm

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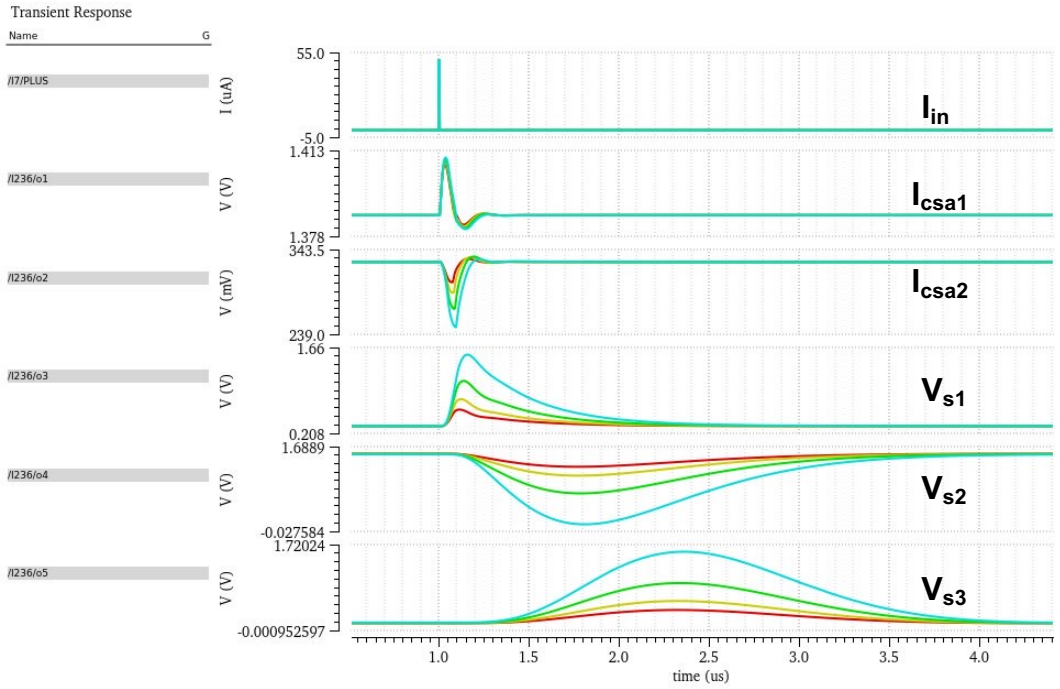
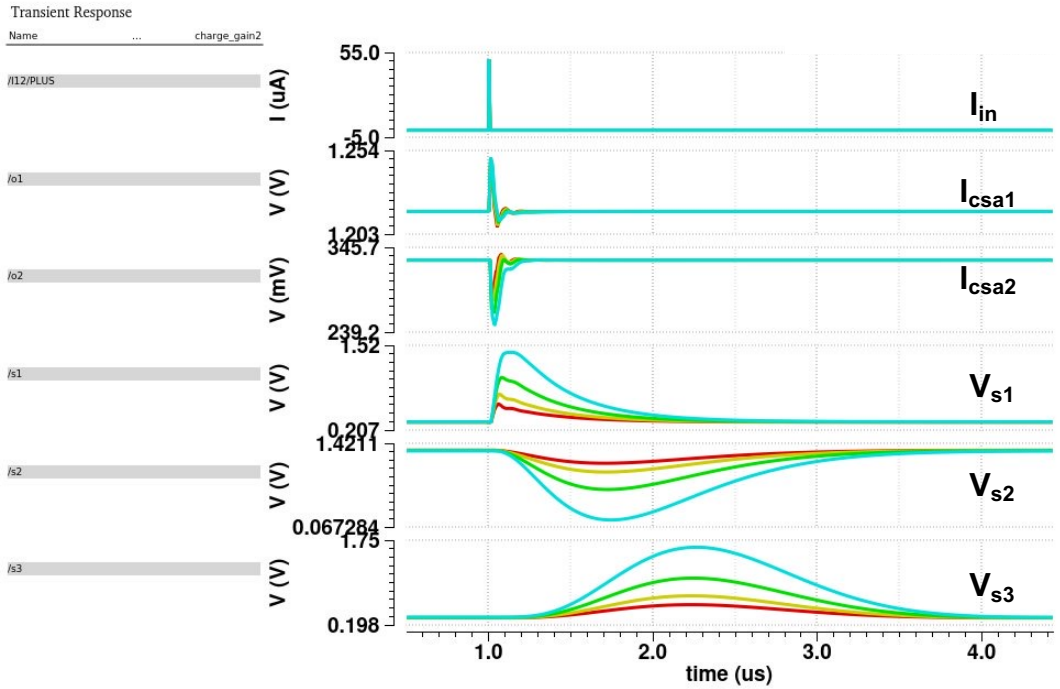
Ref: Angelo Rivetti, Front-End Electronics for Radiation Sensors

Transient response : programmable gain

180 nm



65 nm



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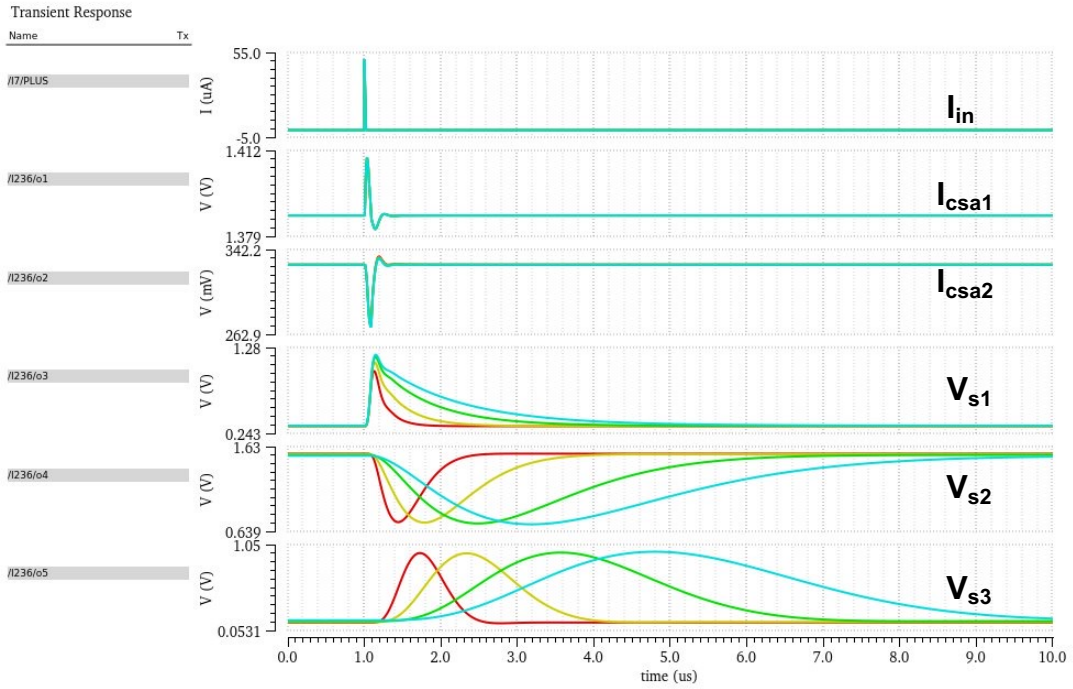
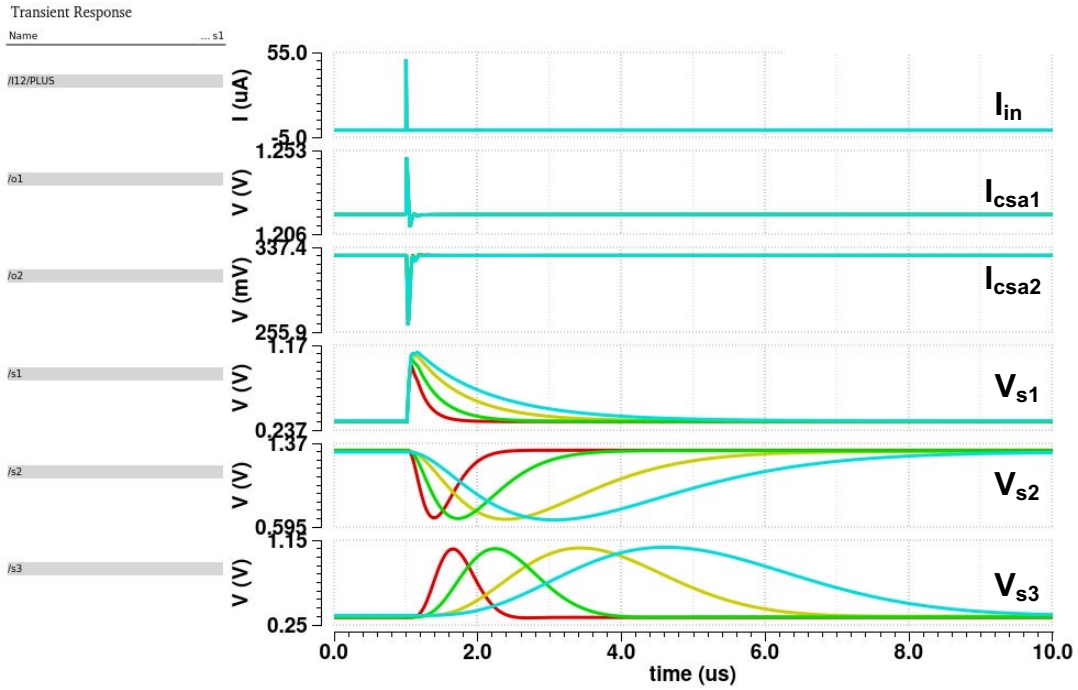
Transient response : programmable peaking time

180 nm



65 nm



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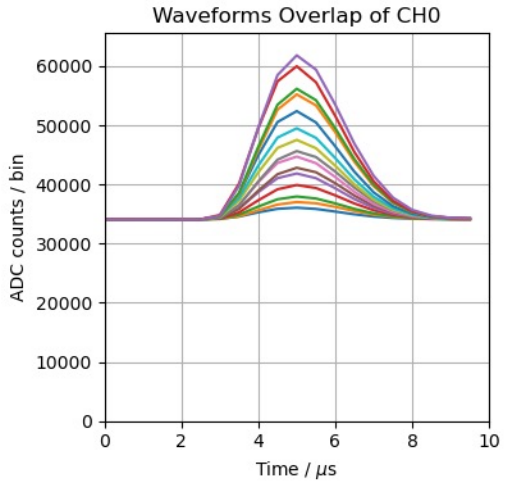
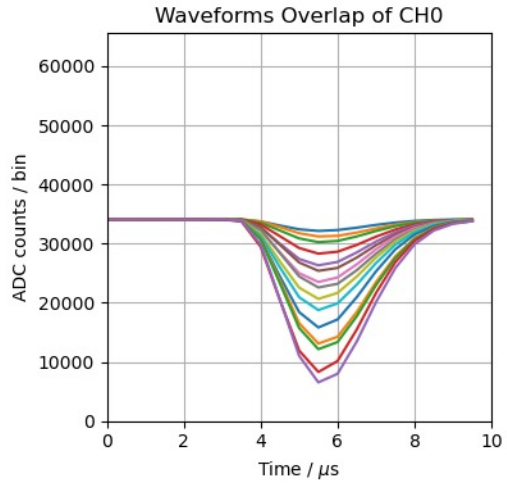
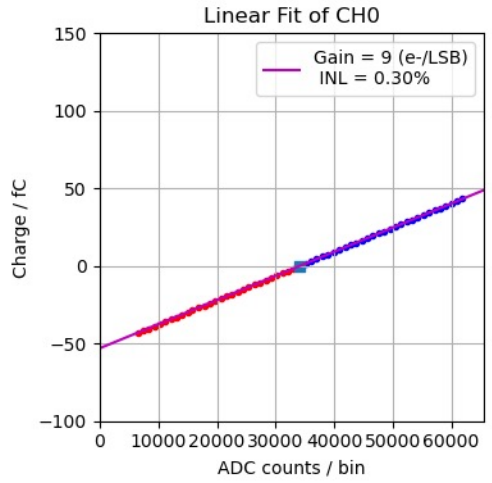
Measured characteristics (P5 – 180 nm)

Charge gain = 9, 900mV baseline, 500pA, T_p = 2μs, ADC 16-bit mode

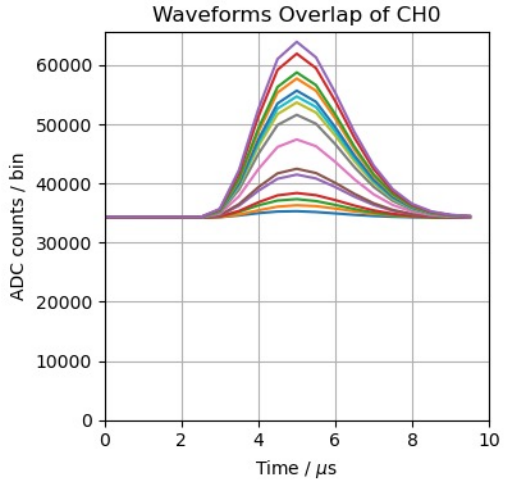
RT

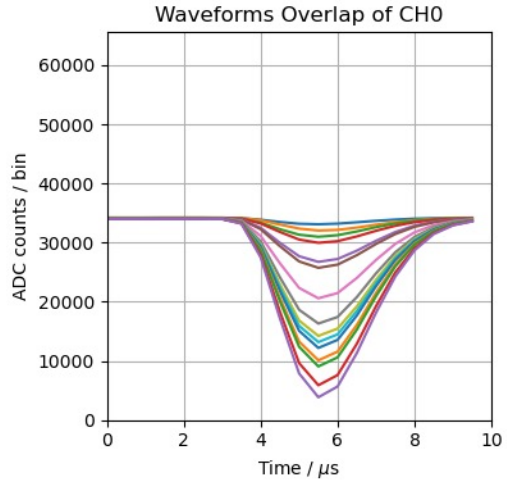


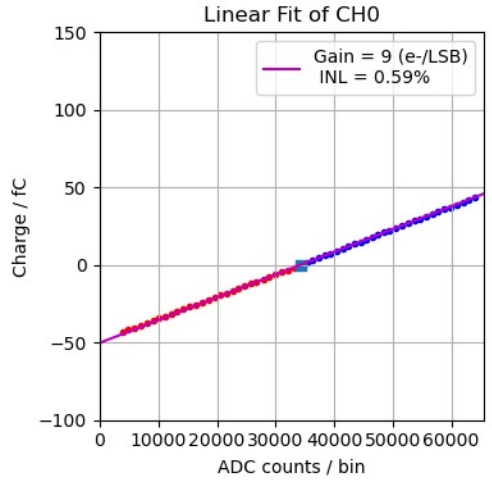




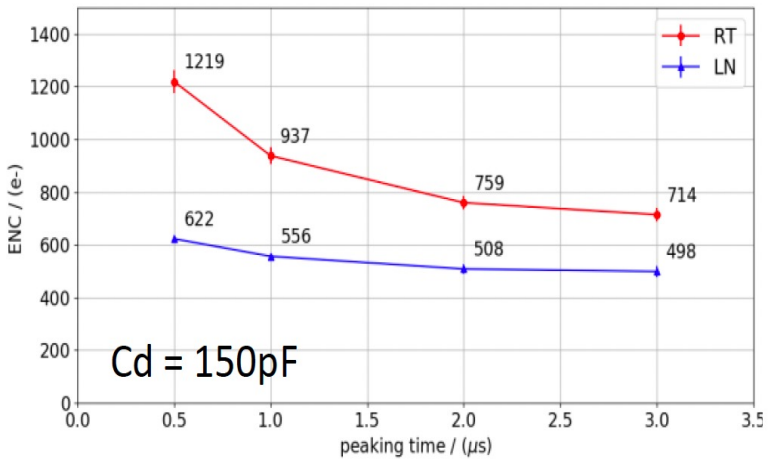
LN2



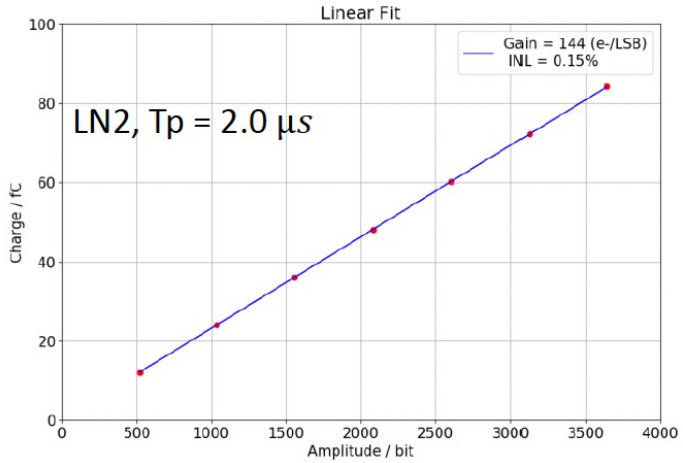




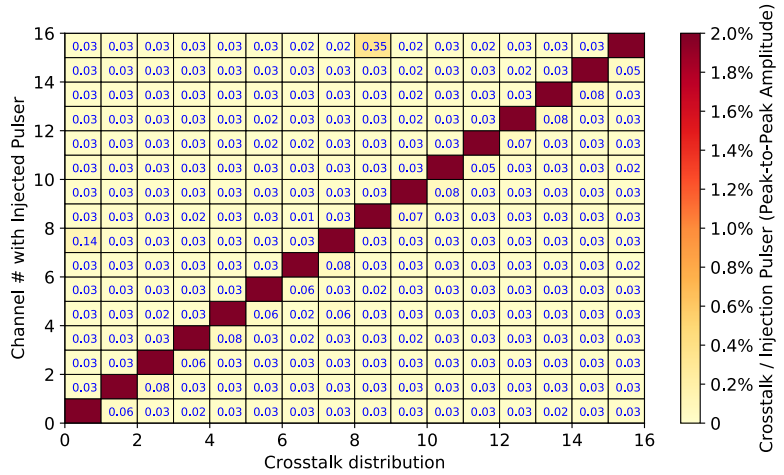
Measured characteristics (P5 – 180 nm)



Low Noise



High Linearity



Low Crosstalk

Noise in 65 nm (simulated) is about 10% lower

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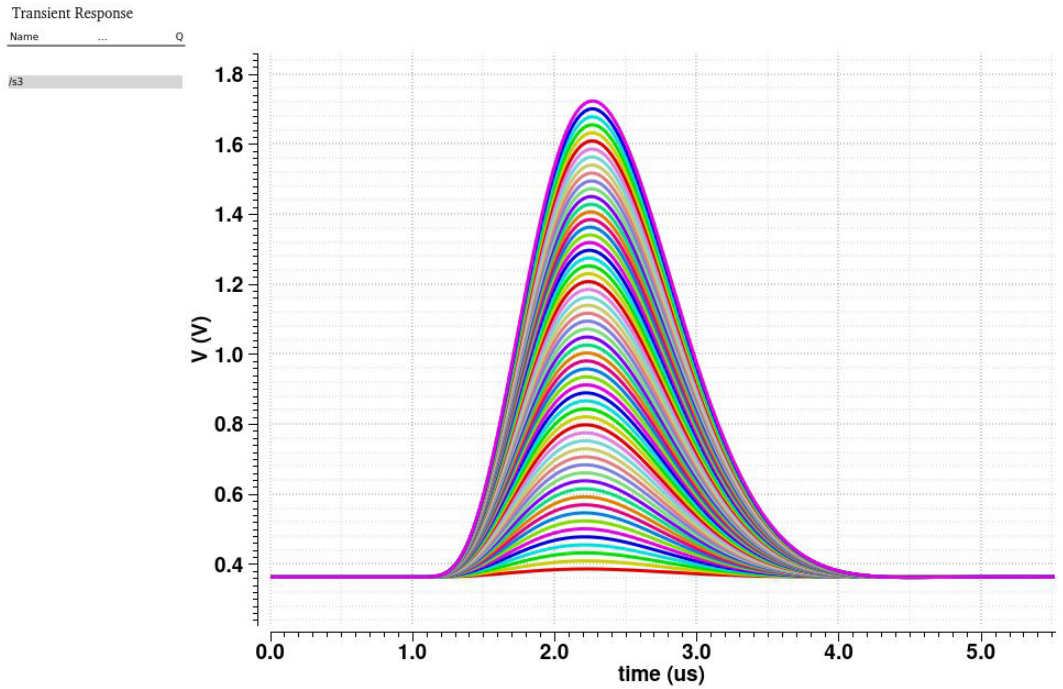
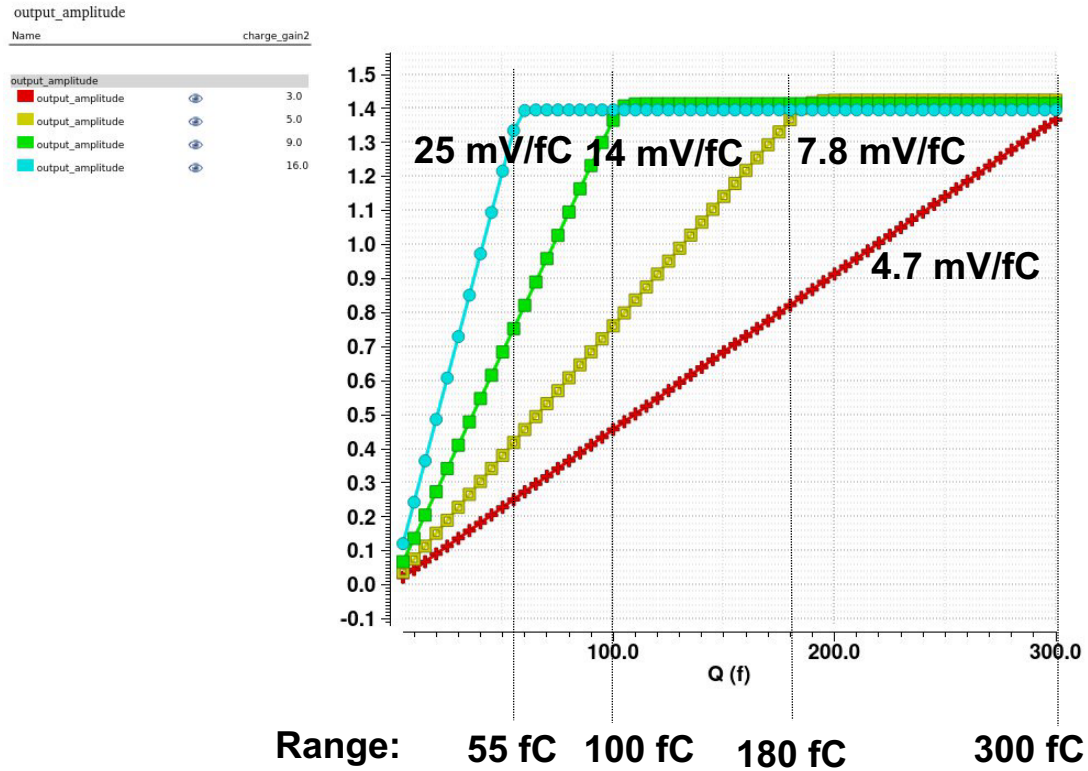
Linearity characteristics (simulated – 65 nm)

Shaper response for charge gain = 3, T_p = 1μs



Output amplitude Vs. input charge



Range: 55 fC 100 fC 180 fC 300 fC

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Next Steps

- Fabricating test structures to obtain better 1/f noise models in 65 nm
- Fabricating the front-end chain in 65 nm
- Checking what is the shortest shaping time achievable with the current architecture
- Customizing the front-end design for shorter shaping times (~ 20 ns, C_d ~ 20 pF) – PIONEER
- Customizing the front-end design to include an on-chip adiabatic capacitor – nEXO (light readout)

Thank you!