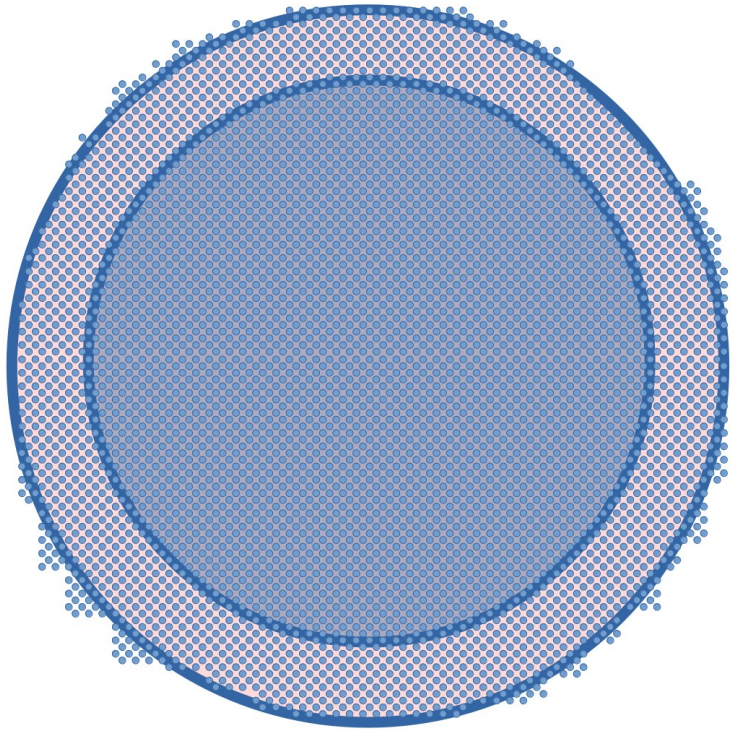
DAQ Status and Overview

Overview

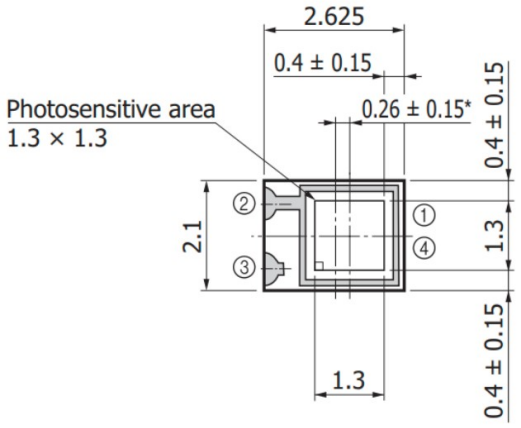
- Current DAQ baseline assumes 20,000 “inner volume” SIPM channels requiring digitization with a further 20,000 being summed together at a ratio of 16:1

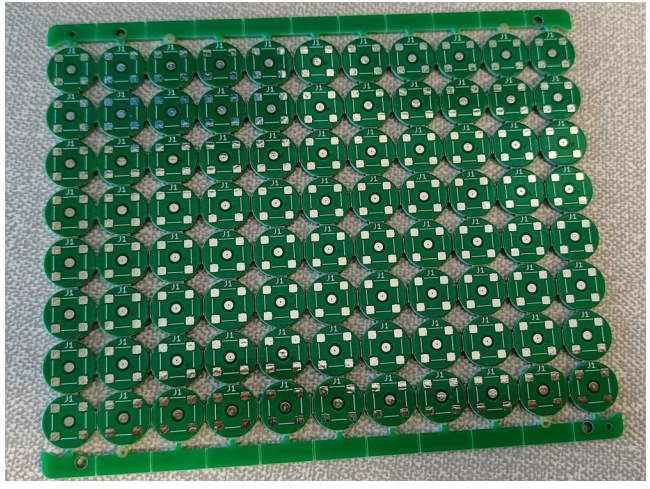


Status

- Researching and interfacing with ASIC vendors and suppliers to see what options are available
- Currently designing small scale demonstrator and test parts for evaluating solutions

SIPM

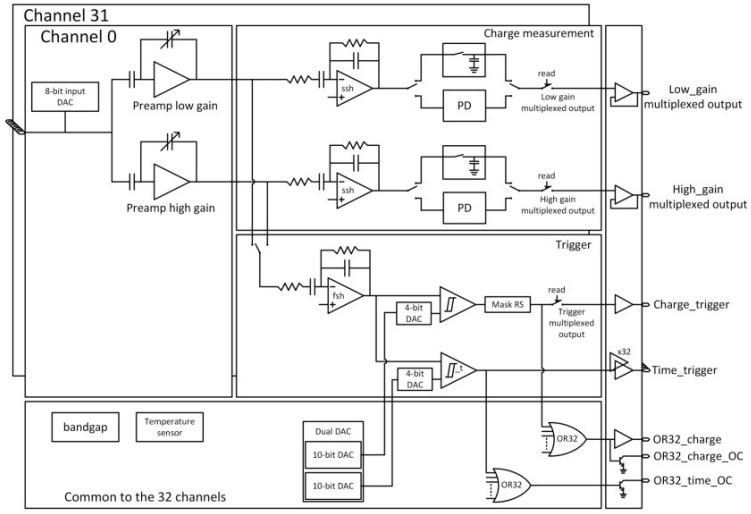




- Current SIPM standard for use in the detector is the S13360-1375PE from Hamamatsu
- Update of the previous uSiC PCB concept for SIPM to be soldered to be connected to by a MCX connector
- Initial test boards made to support mechanical design testing, requires assembly and testing

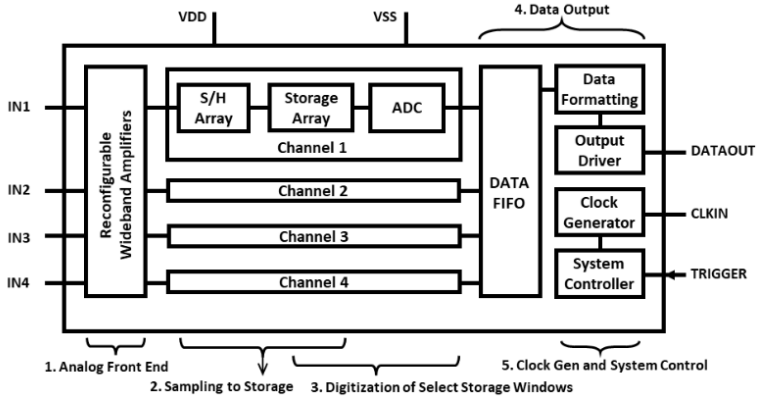
Digitizer: Citiroc-1A

- 32 channel ASIC that can perform charge integration or photon counting operations
- 100KHz all channel charge integration rate, 20MHz independent photon counting rate
- Charge integration measurements sensitive to single p.e. without external amplification



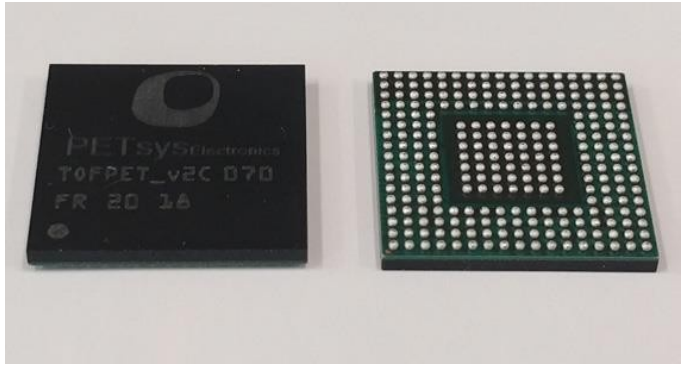
Digitizer: HDSoC V2

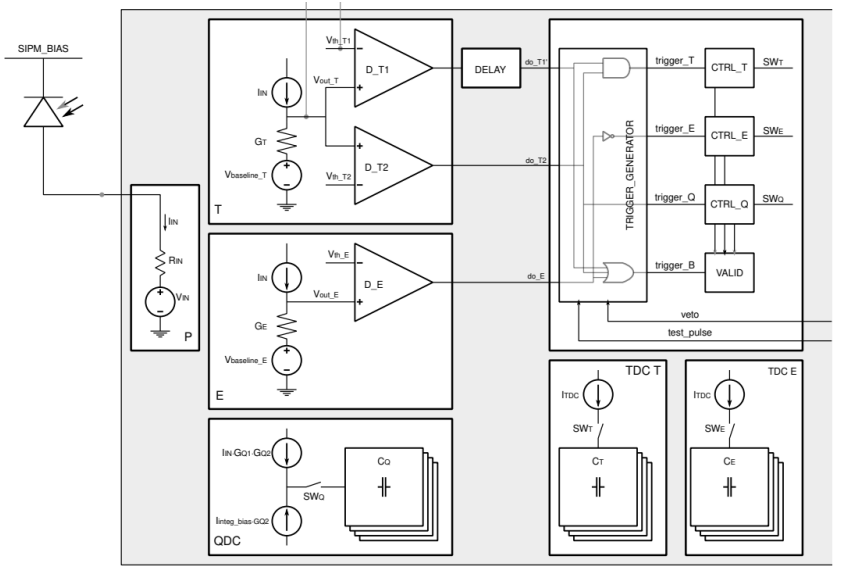
- 64 channel waveform digitizer
- Features flexible channel memory buffer for samples that allow for changes in up to 2uS event recordings
- Can self trigger or exports all channel trigger states every 100nS for logic interpretation and trigger decision
- Flexible trigger options and ROI trigger mode where internal activity detector only digitizes sample block in memory deemed to be valid event signal memory
- 220KHz single channel deadtime-less event rate, 14KHz all channel, (this varies with the number of samples read out)
- V2 evaluation board to be evaluated at Penn State



Digitizer: TOFPET2

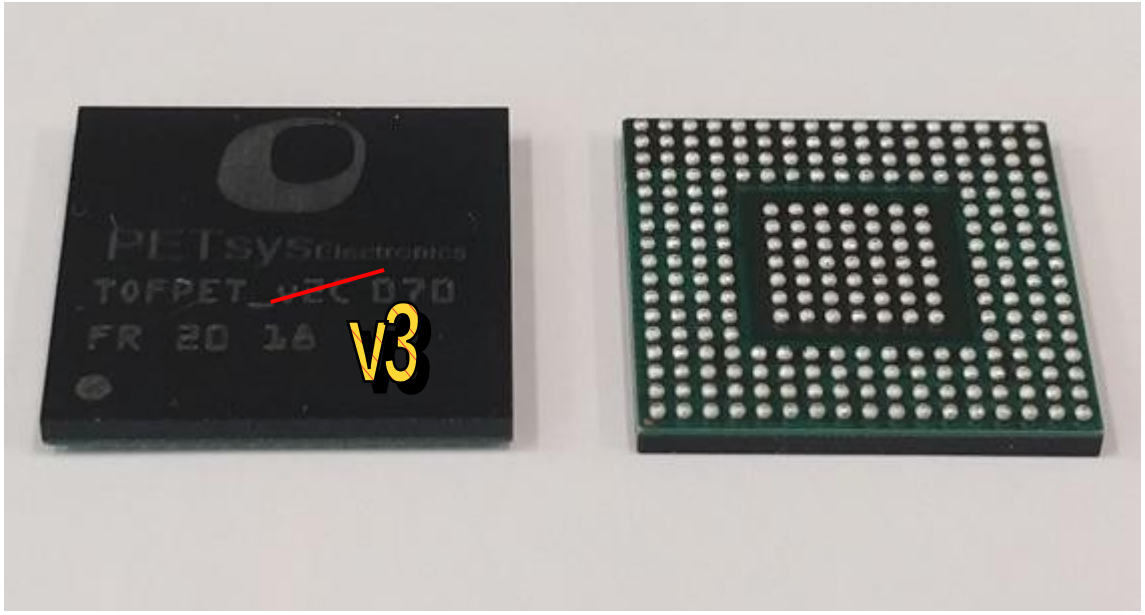
- Can perform either charge integration or time over threshold measurements across 64 channels
- 500KHz event rate per channel, 32MHz event rate per ASIC
- Requires external signal amplification to use charge integration measurement at single photon level
- Used extensively at Sussex as part of the wider PETsys DAQ system , (see recent LiquidO Sussex cube talks from Nicolo/Jess)





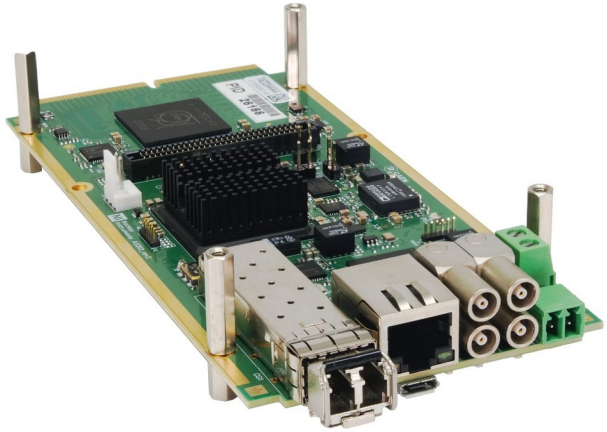
Digitizer: TOFPET3

- New version of the TOFPET ASIC potentially available to sample at the end of October
- Features increased sensitivity to work down to single photon level
- Has additional 4 channels to output summed energy across groups of 16, 32 or 64 channels in the chip

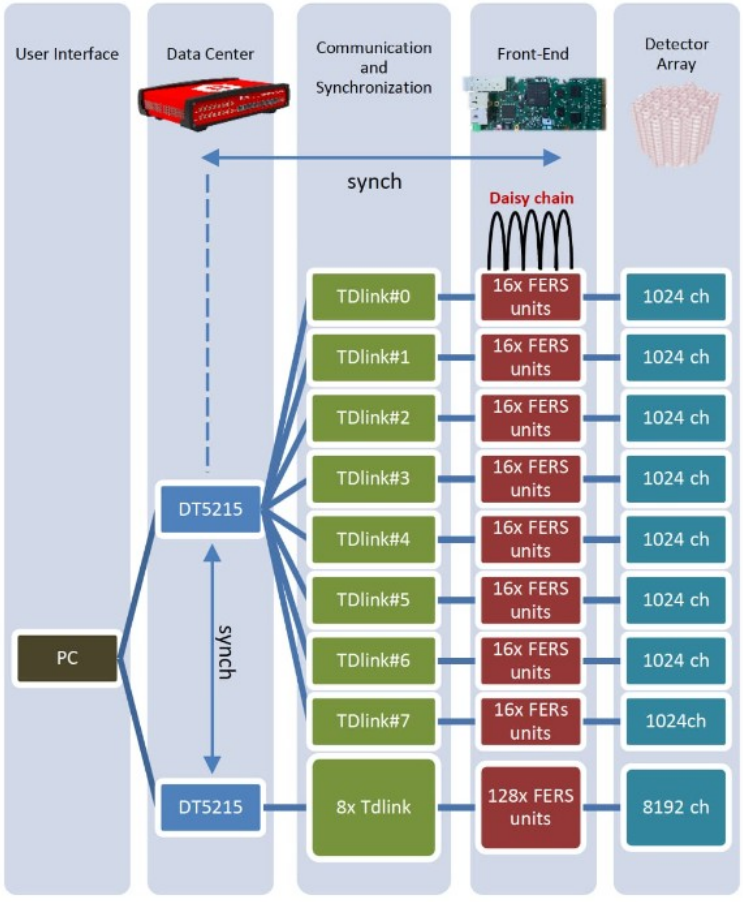


COTS: CAEN FERS

- Scalable readout system with various flavours of FERS readout modules available depending on use.
- A5202 seems most applicable, featuring dual Citiroc-1A ASICs for 64 channel read-in per module
- DT5215 Data Concentrator can be used to synchronise multiple modules, allowing for 8192 channels to be controlled
- Documentation mentions the ability to synchronise multiple DT5215s together to increase scale as needed. Documentation suggests it is a coming feature
- Requires further discussions with CAEN regarding implementations of trigger architectures
- Ability to evaluate FERS at Sussex, RAL and Meinz

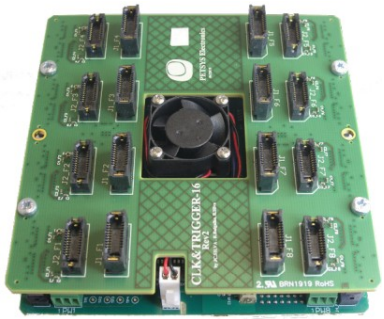


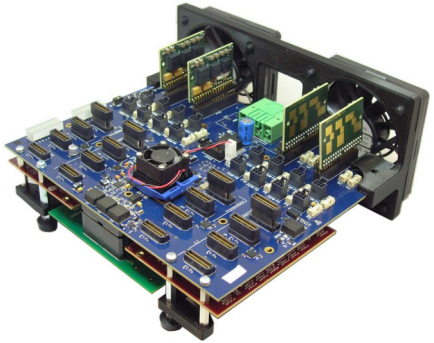
COTS: CAEN FERS

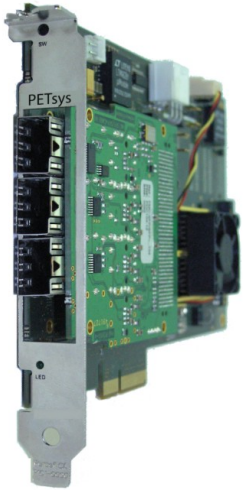


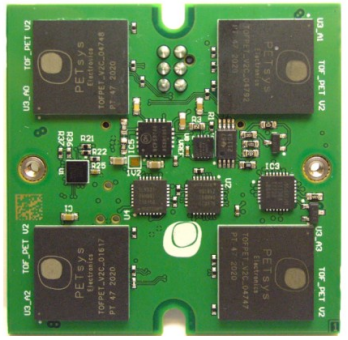
COTS: PETsys DAQ

- PETsys DAQ offers scalable system
- Can be scaled up to over 100,000 SIPM channels with sufficient hardware
- Requires
  - FEM to house ASICs
  - FEB/D for FEMs to connect to
  - Clock and Trigger module for synchronising and triggering multiple FEB/Ds
  - PCIe DAQ card for data ingest
- Different configurations of DAQ hardware can maximise certain aspects, (high event rate, more efficient use of hardware, etc)
- Access to system firmware can be made available for modifications
- Ability to evaluate some aspects of the DAQ system at Sussex

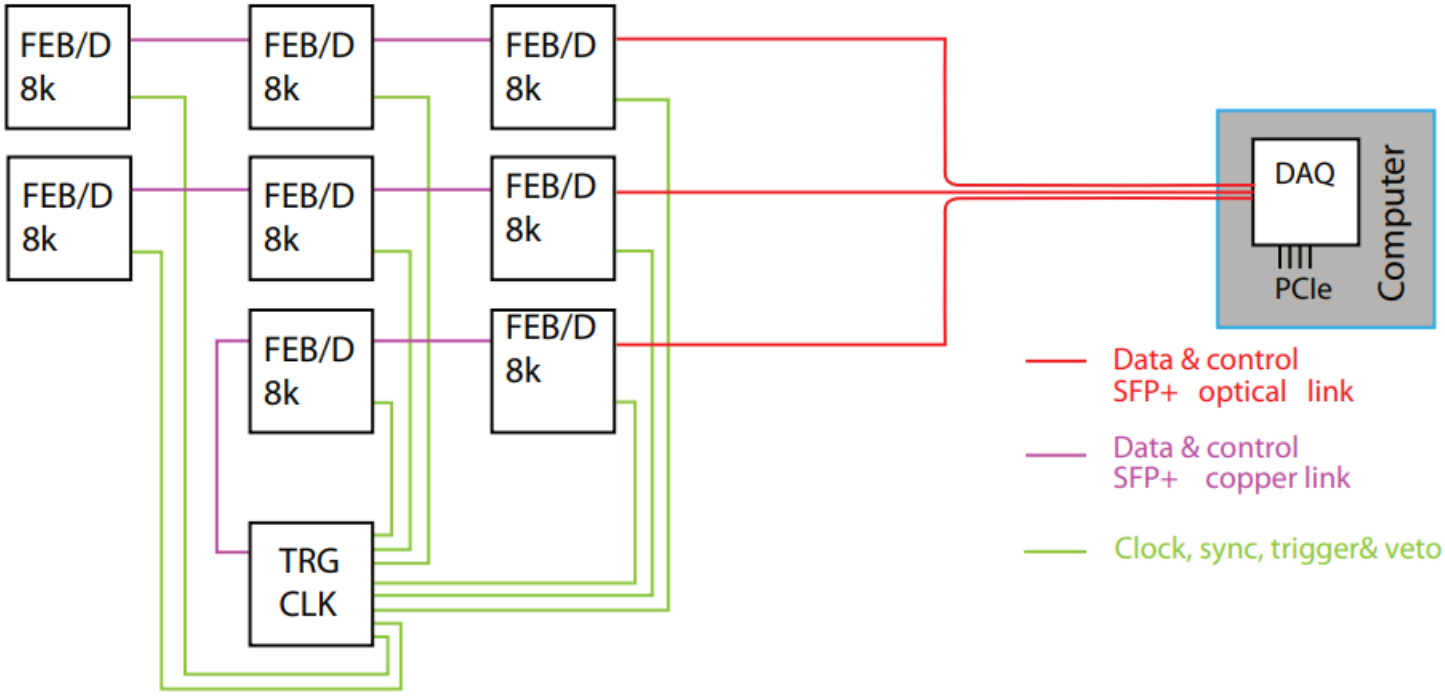




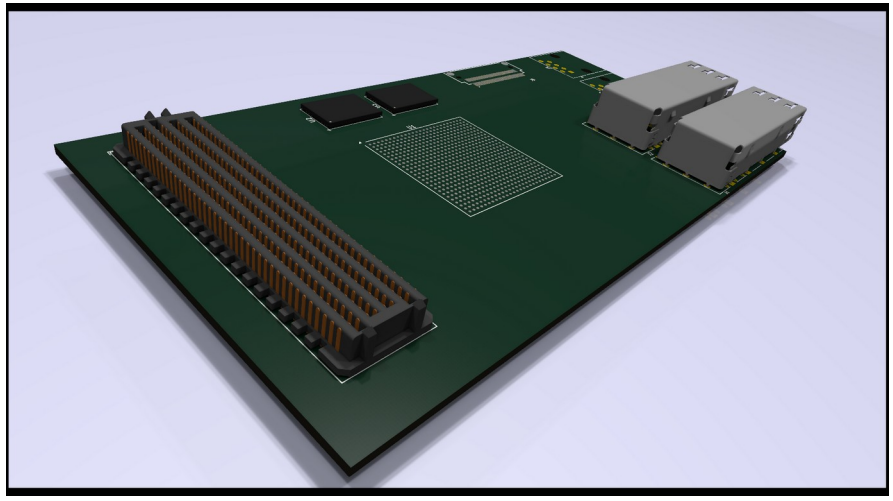


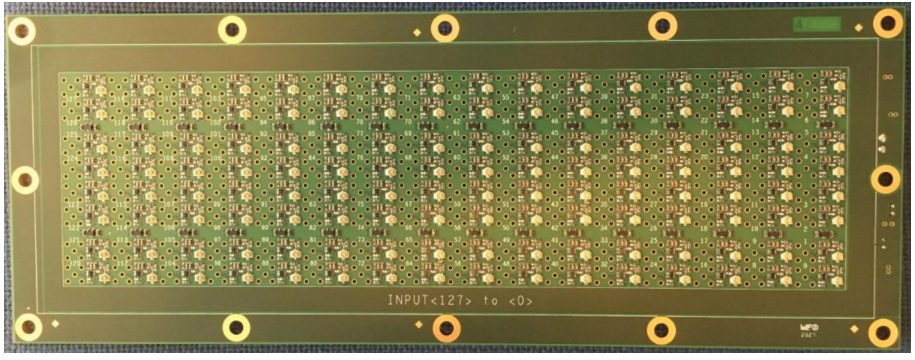


COTS: PETsys DAQ



Custom Implementation





- Currently developing a test platform for digitizer testing
- Based AMD Artix Ultrascale+ FPGA
- Features SFP cages, RJ45 connections and a discrete signal connector
- Features a FMC standard connector. Will allow for FPGA electronics and ASIC electronics to be decoupled and different ASICs to be tested without having to respin entire board
- Developing gain board to allow for multiple SIPMs to be amplified, similar to previous amplifier solution

Design Assumptions

- Available power: 23KW
- Event rate estimates: assuming 2KHz event rate with 1K channels involved per event
- Ability to perform coincidence on either end of fibre a necessary feature to reduce noise triggers
- Assuming ability to cool SIPMs down to reduce dark noise rate