The IDROGEN System

A high data rate acquisition system synchronized by an enhanced White Rabbit node

- IJCLab : Scientific themes : Astroparticles, Astrophysics & Cosmology, Nuclear physics, High Energy Physics, Accelerator Physics, Theory, Heath, Energy
  - Daniel Charlet, Antoine Back, Cédric Esnault, Christelle Soulet, Monique Taurigna, Chafik Cheikali, Olivier Perdereau,*Gaetan Seuillot, *Mathias Vecchio, *Sid Ali Cherrati
- Paris Observatory : Scientific themes : Time and frequency metrology, time and frequency transfer, inertial sensors, space-time reference frames, theory, epistemology
  - LTE : Paul-Eric Pottie, Michel lours
  - Obs Nancay : Cédric Viou

Agenda

- The IDROGEN System
  - Master board
  - Additional functionalities
- Last results on different setup

IDROGEN mother board

IDROGEN Key concepts

- A modular architecture where all signals generated by the master board are
  - synchronous with the master clock: 1-ps stability
  - Time-tagged: 100-ps accuracy
  - Over >100 km distance thanks to an enhanced White Rabbit architecture
- A fully re-configurable syntonic motherboard hosting:
  - Early data transfer at high rate (40 Gb/s)
  - High data rate acquisition boards (4 ch 16 bit 250 MSPS, 2 ch 14 bits 1 GSPS)
  - Arbitrary frequency generator
  - Interface to external digital signals (triggers and interrupts)
- Integration: standalone board or microTCA crate

IDROGEN board v3

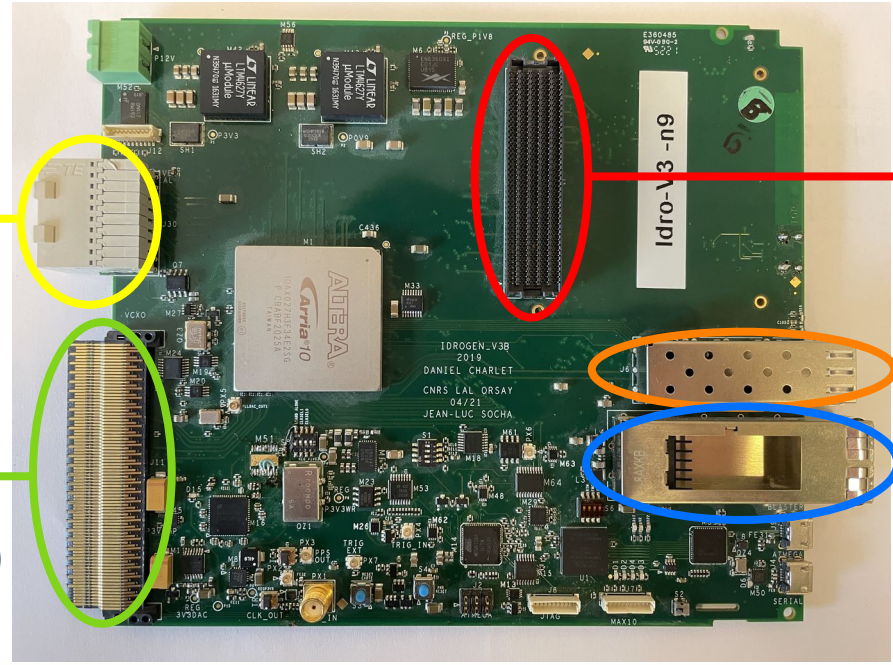
High speed data acquisition & Low phase noise WR node

- White Rabbit Design & development done by IJCLab (based on CERN schematic): Component upgrade and EMC design rules compliant → High stability timing distribution
- xTCA4.0 form factor board → Modularity

- Base on ARRIA 10 FPGA → High data rate transfer
- Standalone capability
- RTM extension boards
- FMC carrier board

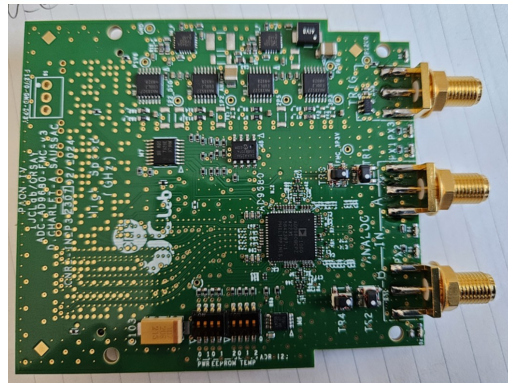
IDROGEN Enhancements

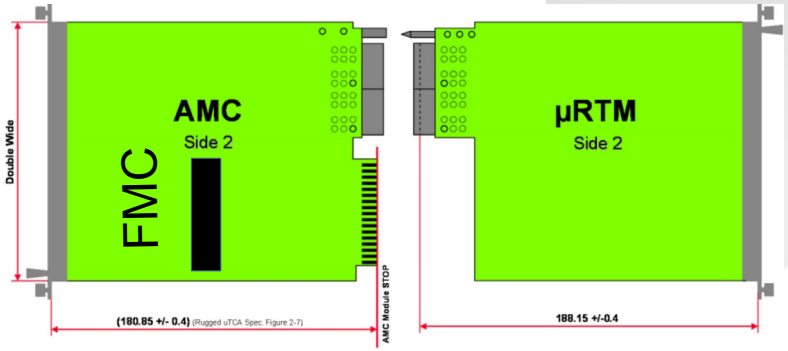
- System frequency
- PLL selection
- VCXO Frequency
- Input frequency for DDMTD
- Tx/Rx routing equalisation



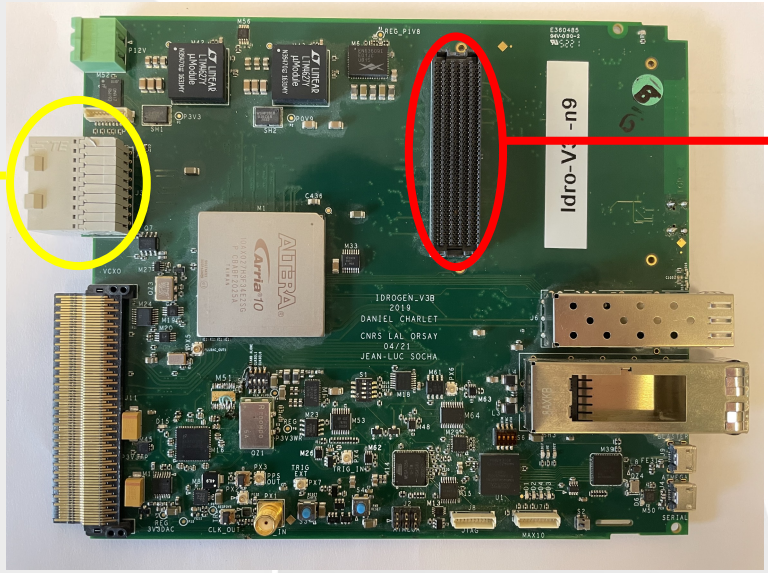
IDROGEN extension boards

- High data rate acquisition boards (4 ch 16 bit 250 MSPS, 2 ch 14 bits 1 GSPS)
- Frequency generator.
- Interface to external digital signals (triggers and interrupts)

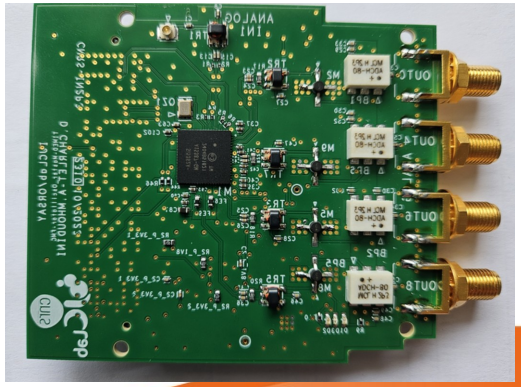




RTM Connector



FMC Slot (ADC, DAC, clock synthesis, ...)

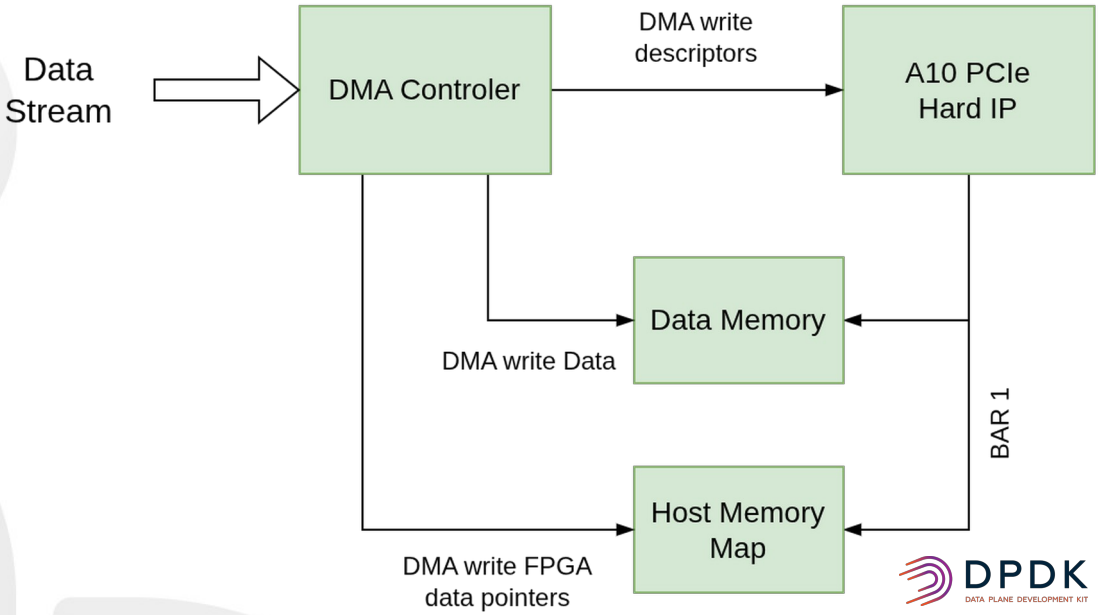


User interface philosophy

- Ensure versatility with early data transfer and high-level language (C, python)
  - Configuration / deployment
  - Signal and data processing in remote server
- Firmware reduced to critical functions
  - White Rabbit
  - Data transfer
  - Low-level interface

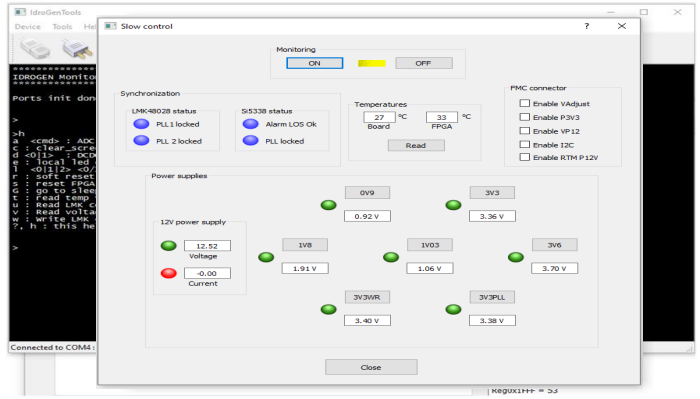
IDROGEN: Firmwares

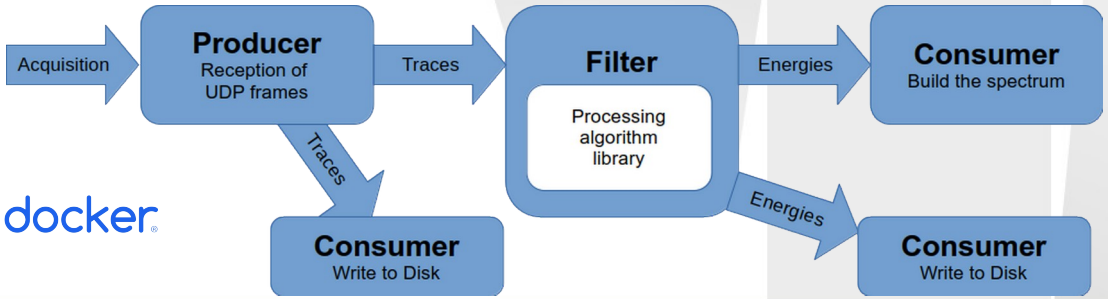
- Data transfer firmware
  - PCI-Express with DMA Gen3x4 (~25Gb/s)
  - GBT protocol (CPPM development for PCIe40)
  - IpBus 1G & 10G portage on Arria 10, from LPSC laboratory developments
  - UDP streamer 1G & 10G
    - Software C, Multi Jumbo frame by event
  - 2 x 10 Gb available, 40 Gb future development
- High speed ADC acquisition
  - JESD204B for (1G/500M/250M)
- Parallel 64 data acquisition
- White Rabbit core v4 & v5 porting on Arria 10
  - Master & Switch (on development)

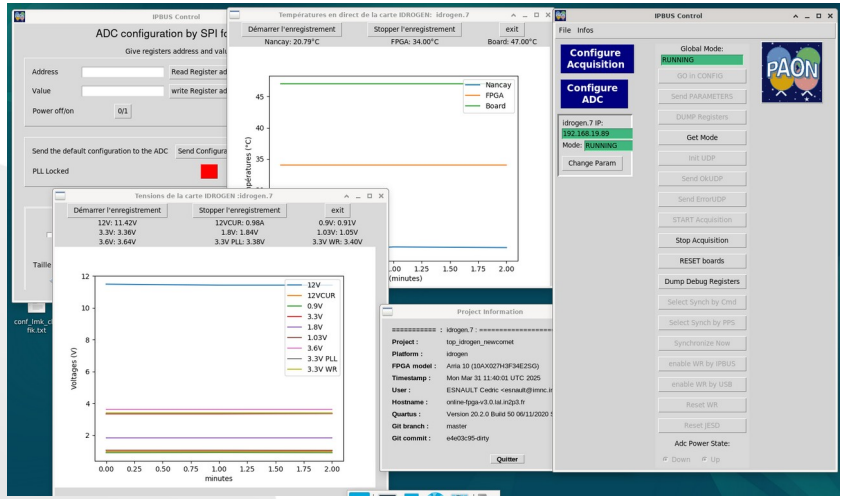


IDROGEN: softwares

- Configuration GUI tools over USB and Ethernet (IPBus protocol)
  - Power, PLL, FMC and ADC configuration
- Monitoring GUI for power supplies and temperature monitoring
- Slow control library and tools (I2C, SPI, WR diagnostic, …)
- Frame viewer
- Acquisition software
  - Based on DCOD framework
  - Implement a generic processing algorithm interface (loading a dynamic library)
  - Based on widely used technologies (Docker, DPDK)







Mechanical integration

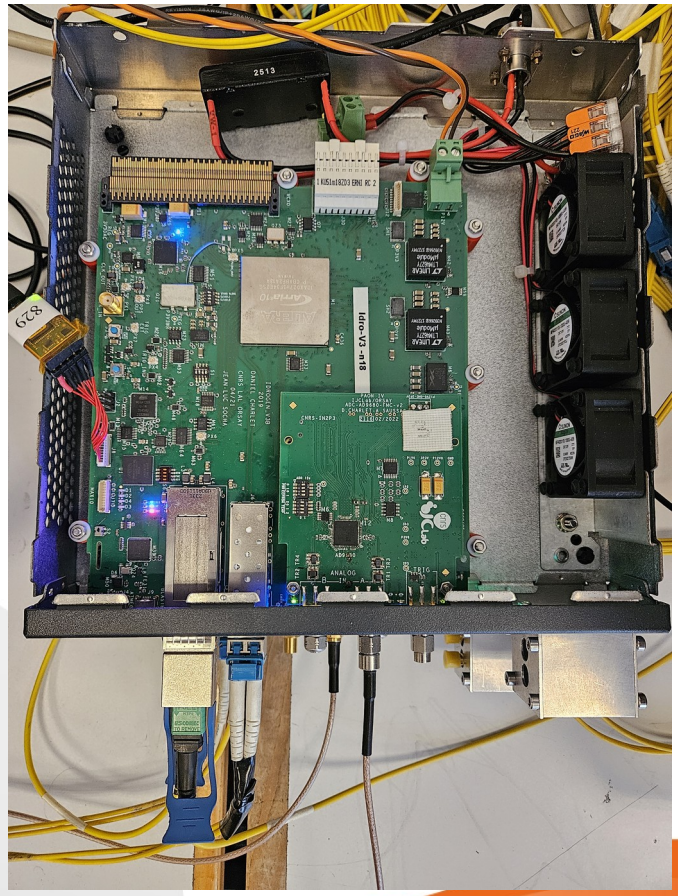
XTCA crate



EMI immune, waterproof, pwr 12v, passive heat dissipation



EMI protection, pwr 24V, active heat dissipation

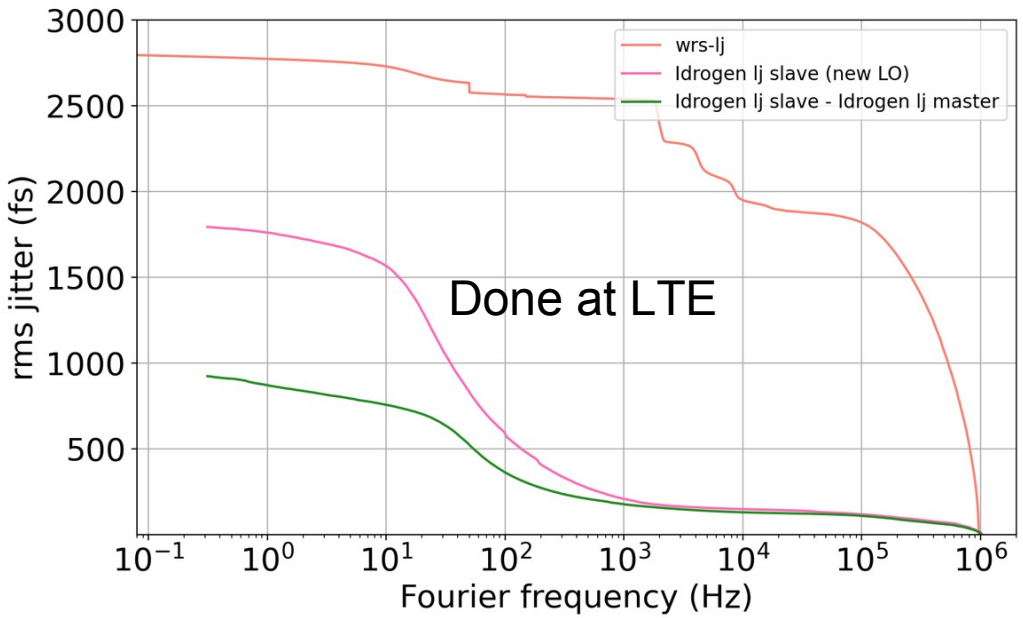


IDROGEN board: Timing performance

IDROGEN board performance: 1-ps RMS jitter

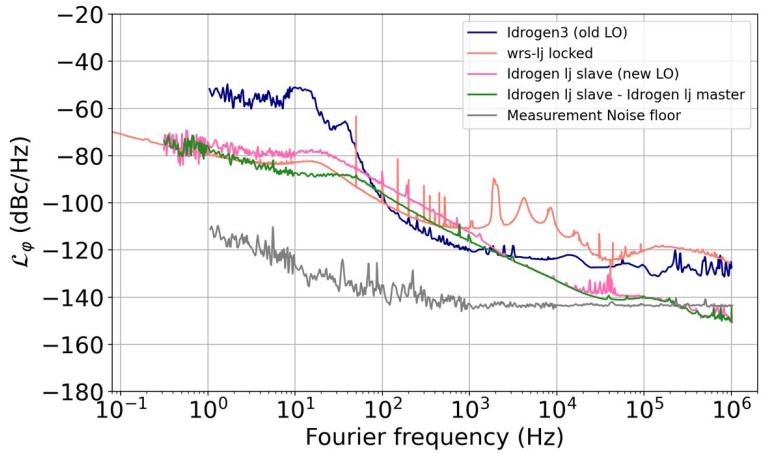
IDROGEN BOARD: 4x better than Low Jitter Switch from Safran

Integrated jitter according to integration range



Variation of lower bound of integration range.
Upper bound fixed at 1 MHz

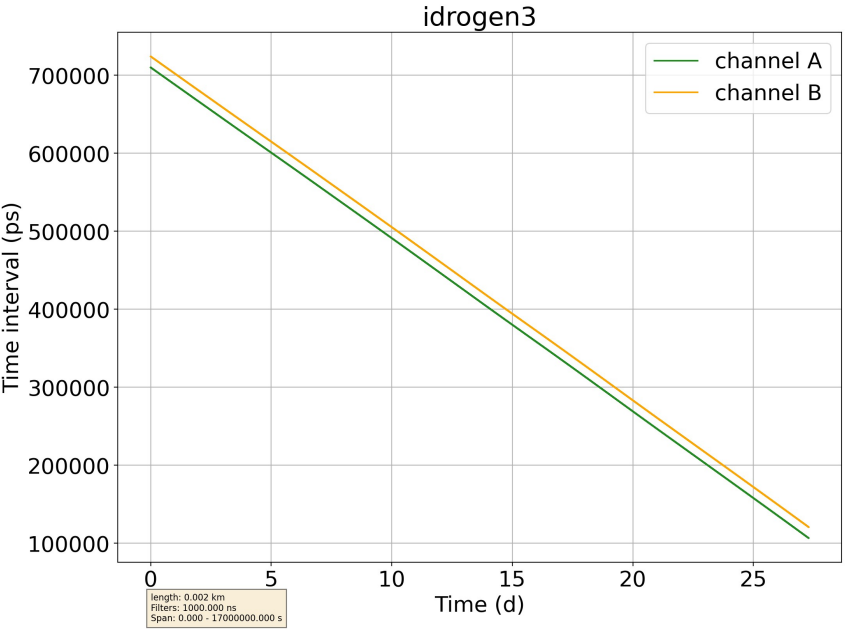
Phase noise measurement

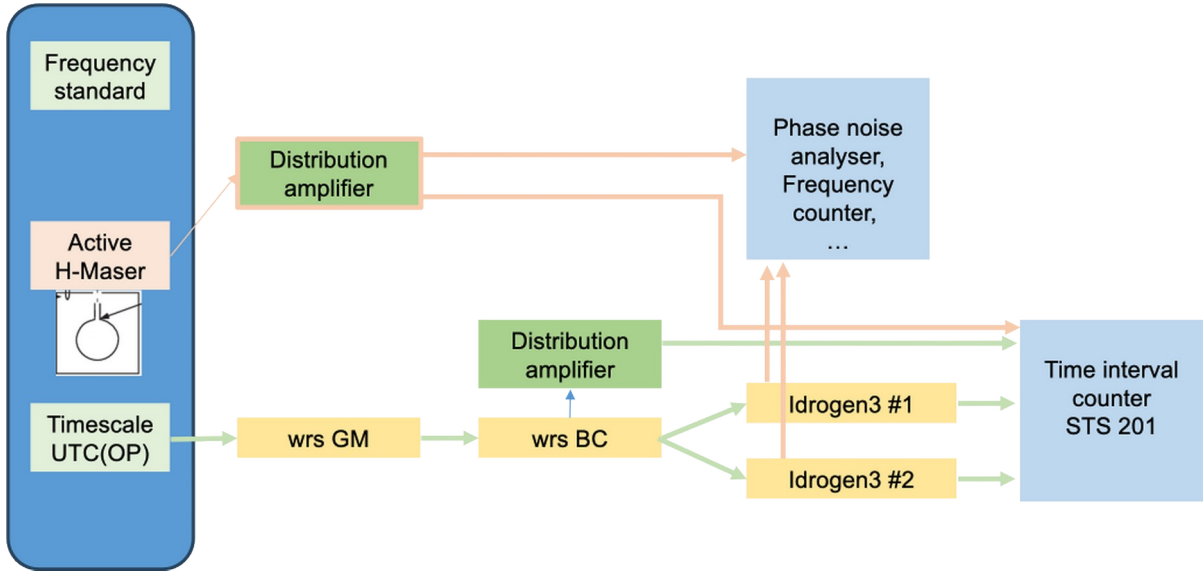


	1	10	100	1,000	10,000
wrs-lj	2 246	2 191	1 984	1 075	1 075
S	1 757	1 557	563	110	110
S-M	866	751	351	94	94
GM	445	439	432	129	129

Table 1: Integrated rms jitter expressed in fs for Idrogen and a wrs-lj, for integration bandwidth up to 100 kHz

IDROGEN board performances

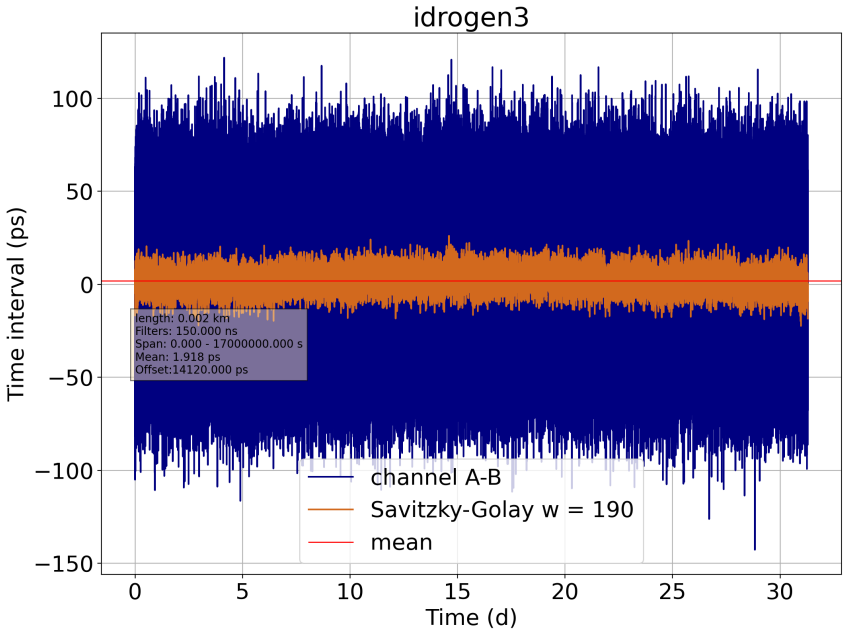


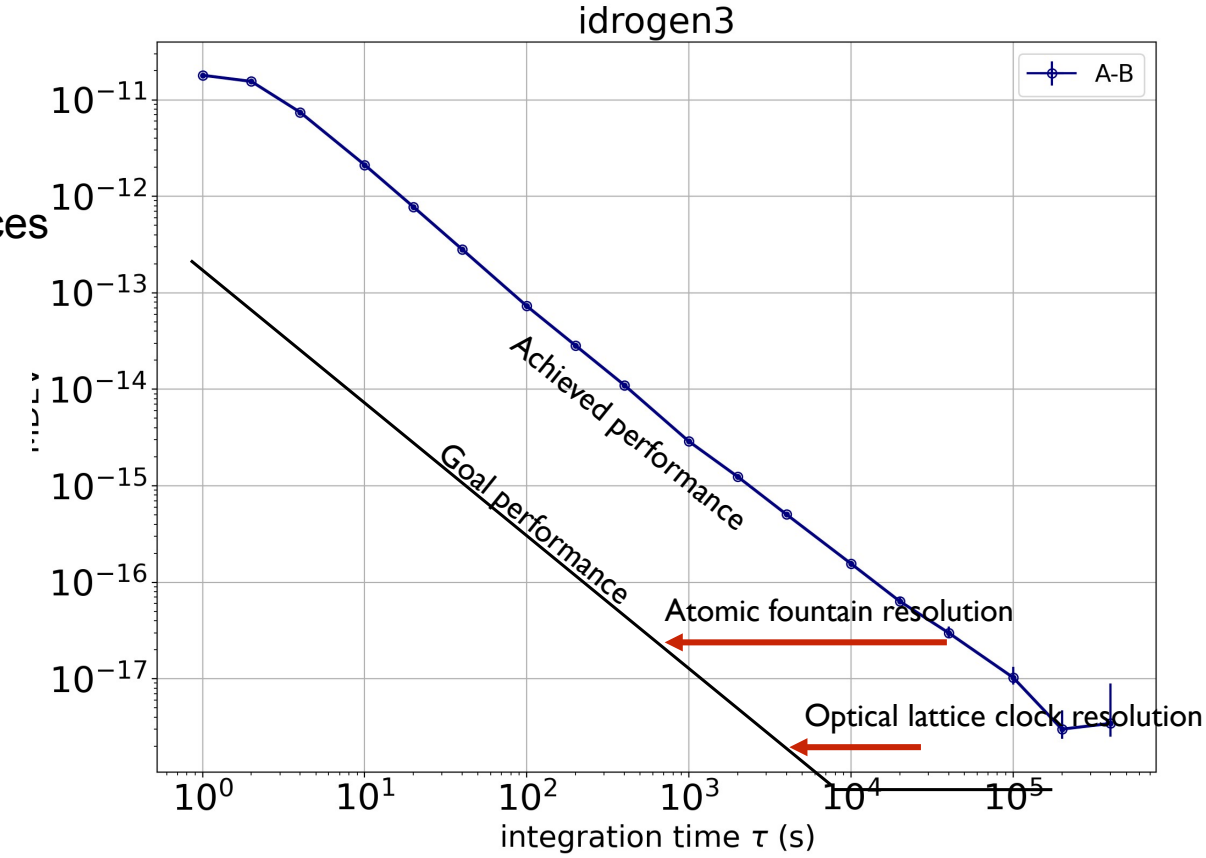


- Measure the time interval between idrogen#1 and idrogen#2 PPS :

IDROGEN board stability : 3e-18 over 30 days

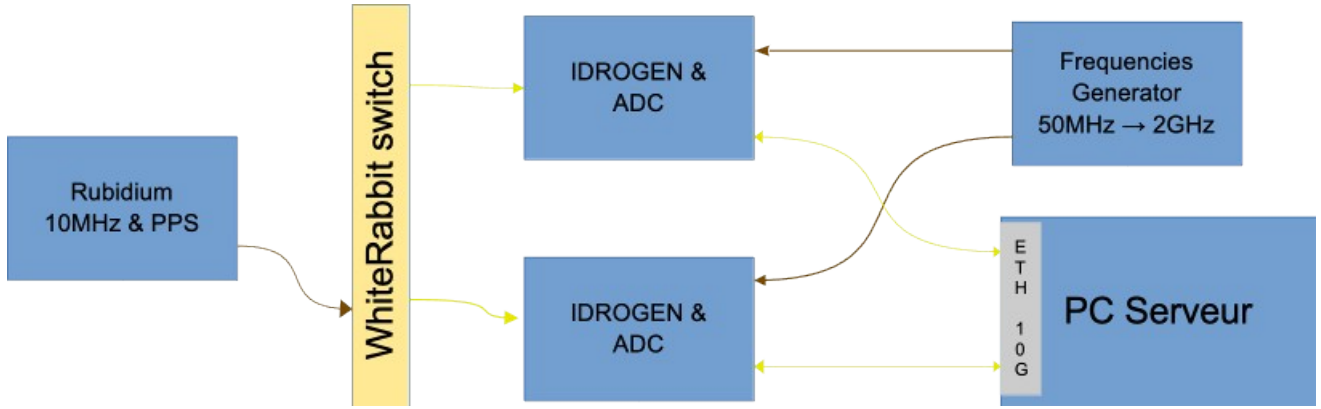
- PPS time difference between two independent IDROGEN3 boards
- Excellent long term stability : ~ 3E-18
- On-going work: improve short term performances
-

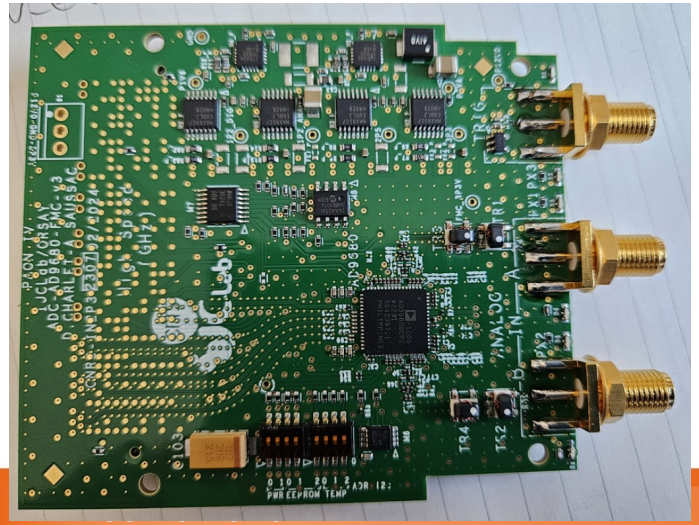




1GSPS ADC board: Synchronization performance

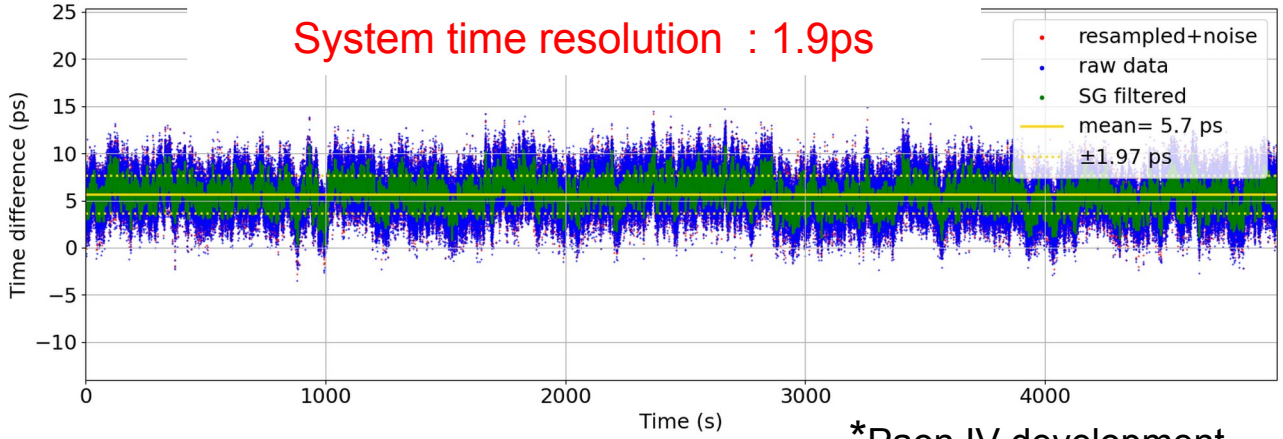
- Bandwidth (single board):
  ~500Mhz (1GHz → 1.5GHz)
- 2 IDROGEN boards synchronized by WR
- 2 channels 1GSPS 14b ADC
- Same RF signal (312.5MHz) split on boards
- FFT 8k point
- Cross correlation





Two IDROGEN board

System time resolution : 1.9ps



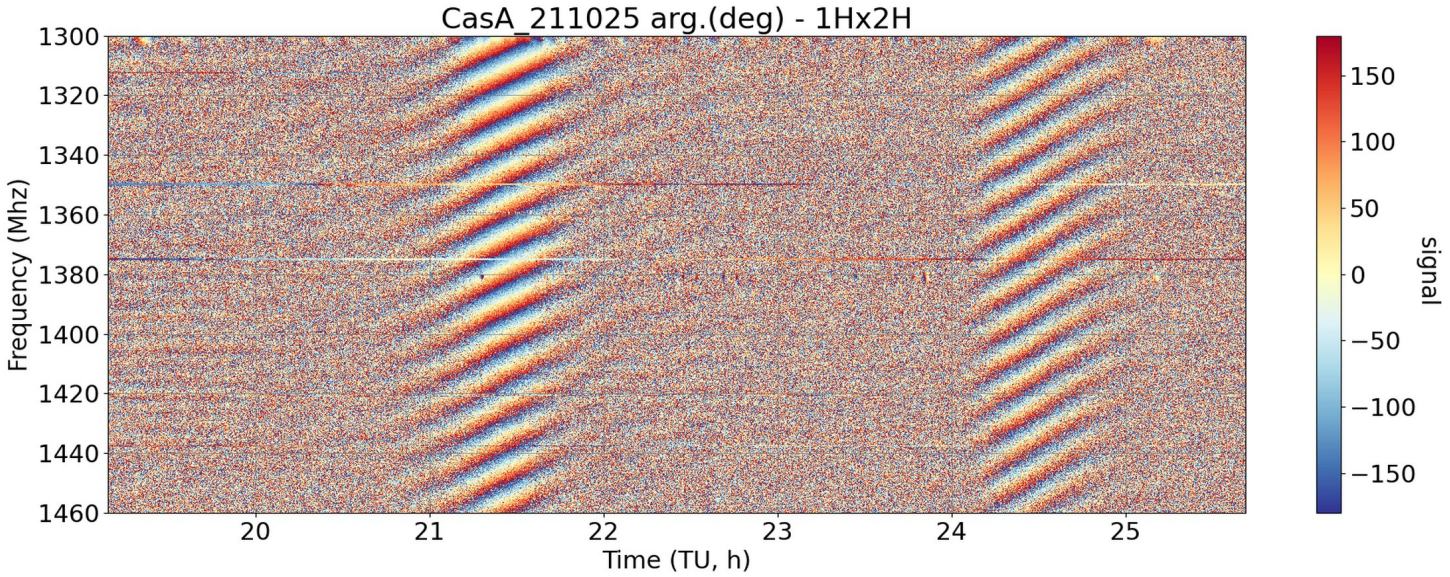
*Paon IV development

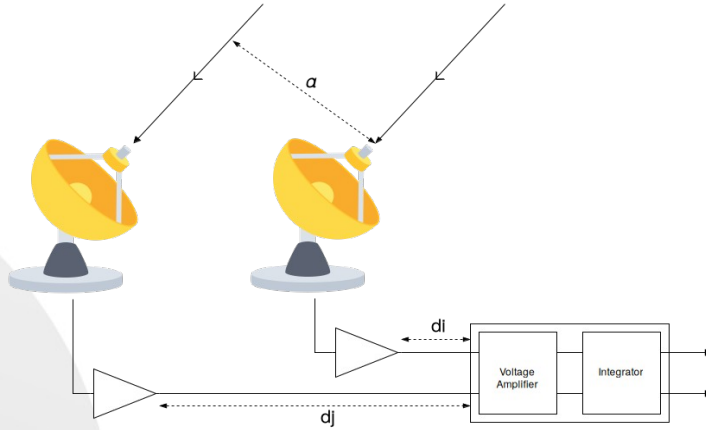
Applications to interferometry

PAON IV Radio Interferometer

- Nancay Observatory
- Acquisition by IDROGEN board and ADC 1GSPS
- Phase difference between 2 antennas
- Synchronization by REFIMEVE network
  - Paris observatory UTC(OP) connection
  - **Fiber link length ~ 300km**







Typical configuration of radio interferometer

IDROGEN interferometry for CTAO?

- Hardware :
  - 2 IDROGEN-V3 + 1GSPS boards with mechanic integration in test at IJCLab
  - Complete setup will be test on CEA camera for the end of 2026

- Firmware
  - 40Gb eth: IpBus and UDP streamer (on development)
  - RDMA transfer
- Software
  - Data transfer for 40Gb
  - Online signal processing
  - Configuration by IpBus 40Gb
  - Debian deployment, Docker deployment Q1 2027

NectarCAM

Clock synthesis: 10 kHz to 2.75 GHz, phase noise < 1.7 ps RMS

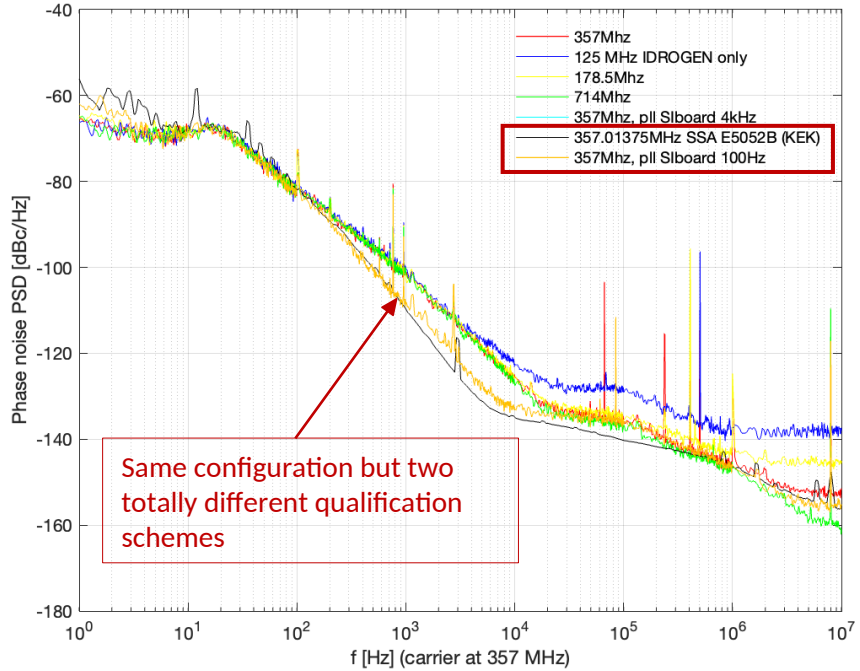
Fractional PLL (FPLL) for accelerator synchronization (SI5362)

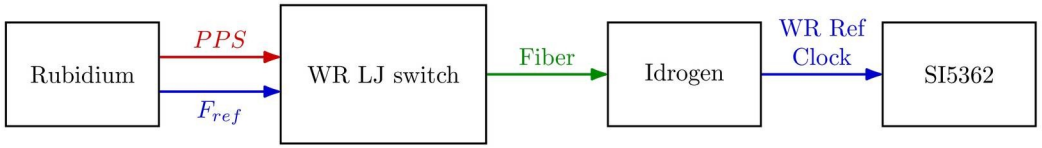
- Generate frequencies, disciplined by WR clock, from 10kHz to 2.75GHz, with 1 Hz resolution.

SI5362: Phase noise measurement

- Tests performed at IJCLab and KEK (SuperKEKB and ATF);
- Phase noise measured for various different output frequencies and input filters, re-scaled at 357 MHz: 1.7ps RMS jitter;

RTM additional board Q1 2027







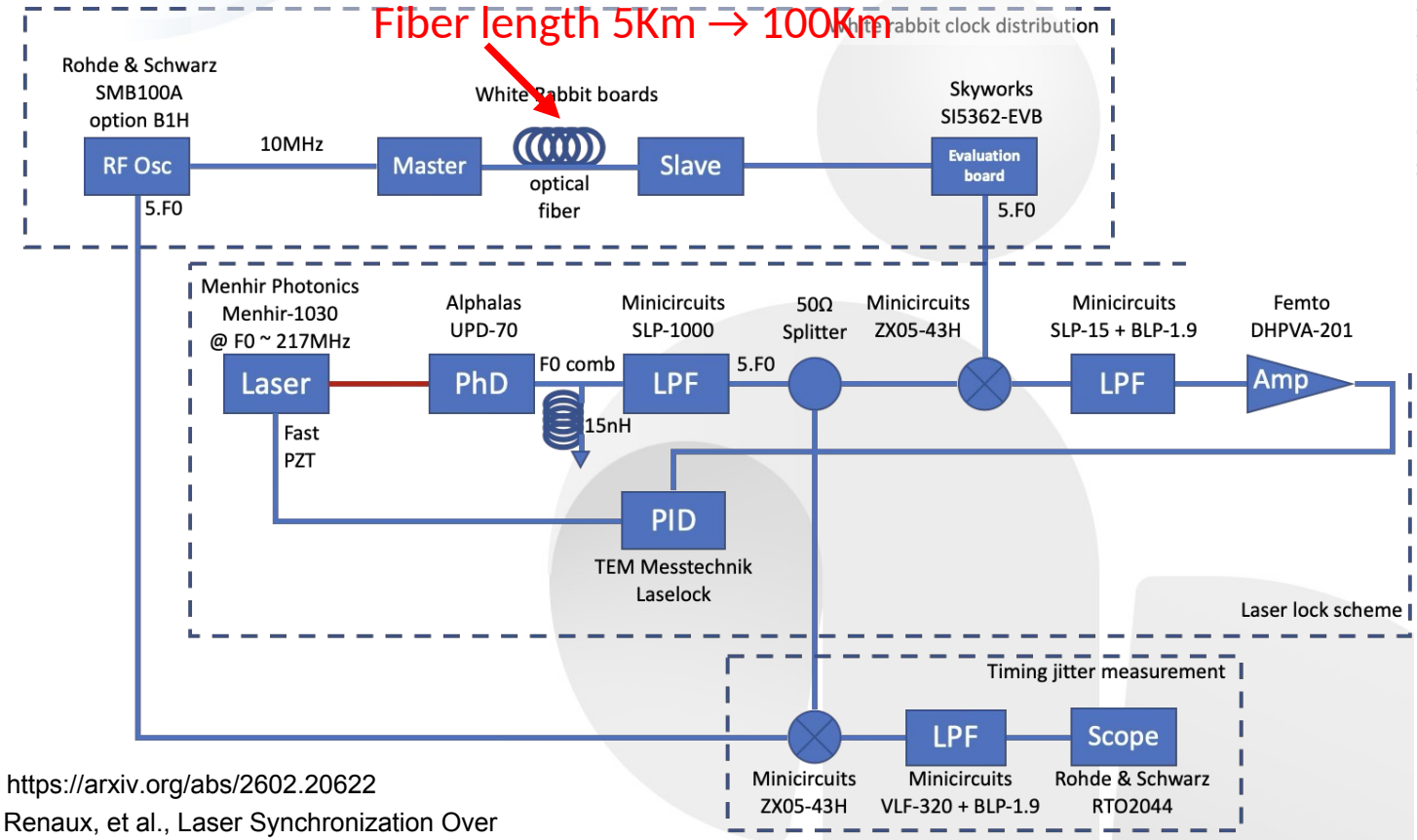
Funded by the European Union

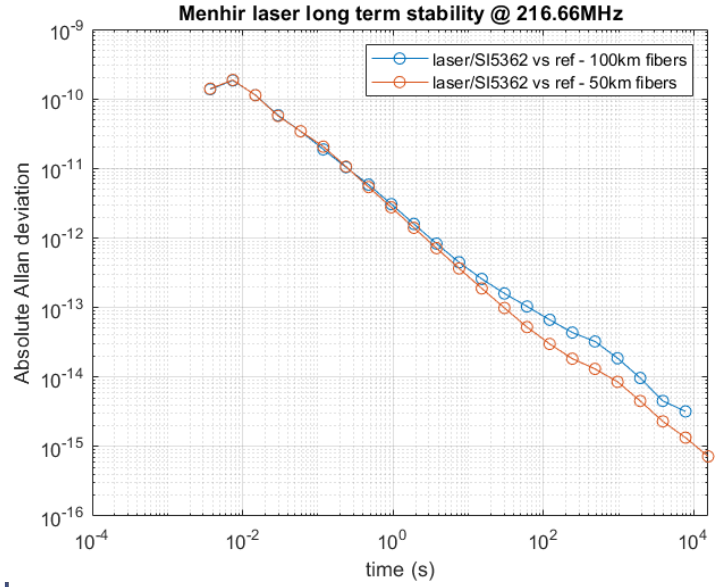
The research leading to these results has received funding from the European Union's Horizon Europe MSCA under grant agreement no. 101086276

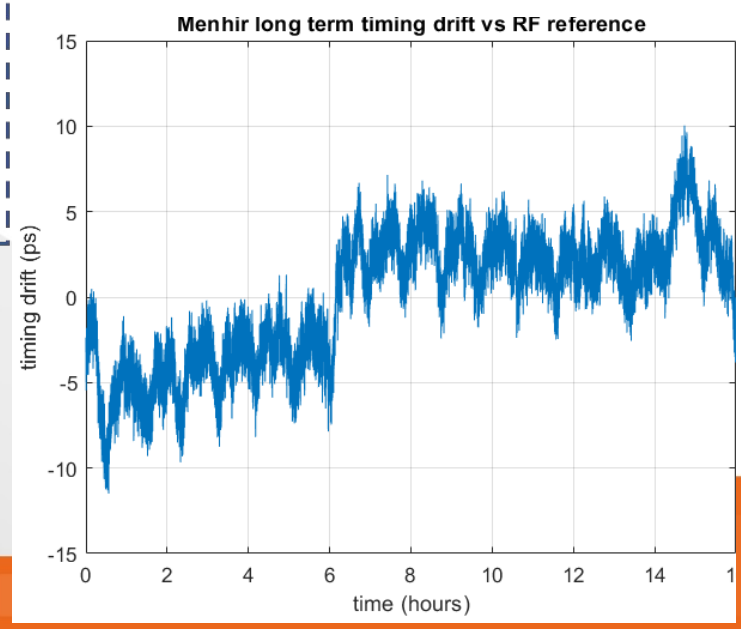
Laser synchronisation > 100 km

IDROGEN 1 : GM → IDROGEN 2 slave

Fiber length 5Km → 100Km







https://arxiv.org/abs/2602.20622

Renaux, et al., Laser Synchronization Over One Hundred Kilometers With Stability at Picosecond Scale, IEEE TIM 2026, doi:10.1109/TIM.2026.3706219, preprint, doi:10.48550/arXiv.2602.20622

IDROGEN: roadmap and future directions

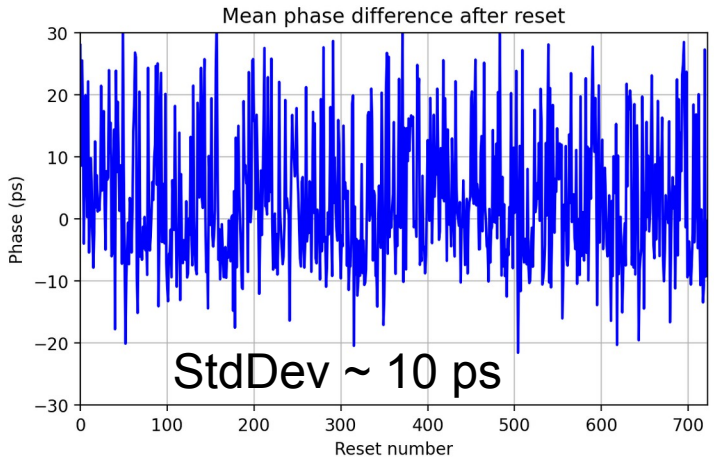
- **IDROGEN_V4**
  - Prototype Q4 2026, mass production Q1 2027 (if components are available …)
  - Replacement of obsolete components
  - Selections of new components for better performances
  - Versatility Improvement
- FMC-AD42JB69-V2 (in cabling)
  - 4 channels 250MSPS 16bits
- FMC-ADC 3GSPS (development Q1 2027)
- **Hardware**
  - FMC-3.6GSPS 2 channels 12b. Prototype Q1 2027:
  - 40Gb on development (IpBus access and UDP streamer)
  - 40 Gb RDMA

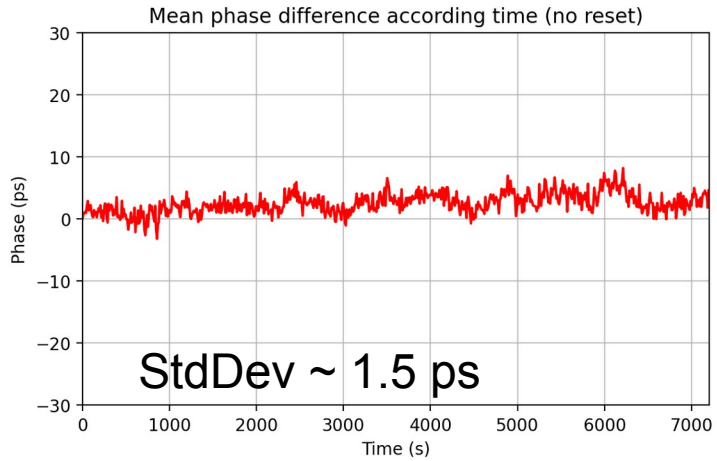
- **White Fox** IN2P3 R & T project (Highly improved White Rabbit)
  - Development with LTE
  - Sub 100-fs performance (prototype in development)
  - RTM extension of IDROGEN board

- **Performances Improvements**: (ongoing development)
  - short term performance:
    - WhiteRabbit software configuration
    - Firmware
  - long distance stability > 50Km
- IDROGEN_v5
  - New FPGA familly AGILEX
  - 100Gb RDMA
- 10Gb/s White Rabbit firmware

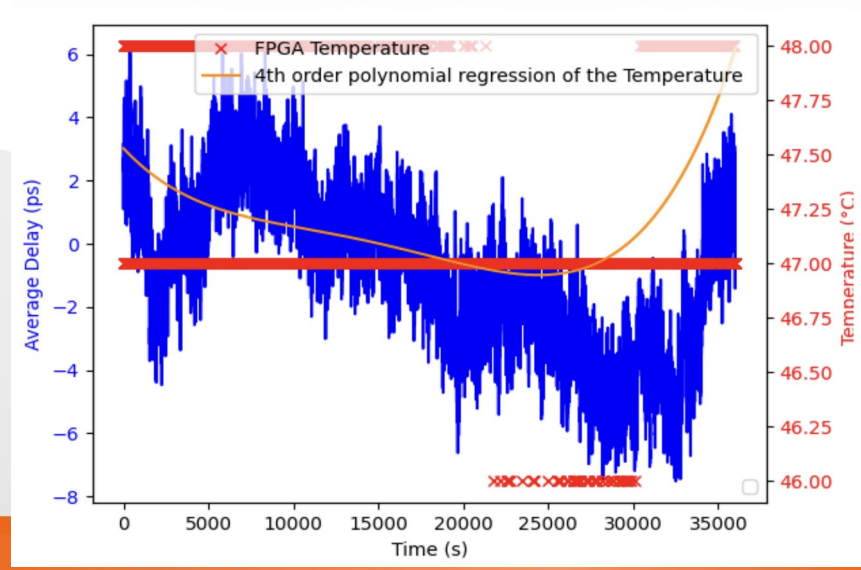
IDROGEN and WhiteRabbit improvment

- **Phase after reset**
  - Measure at 1GHz → ~30ps rms
  - Modifications of the WR firmware and software





- **Temperature influences**
  - We are dominate by the temperature of the setup
  - The thermometers are not sensitive enough → new one on V4 version.
  - Integration of temperature correction

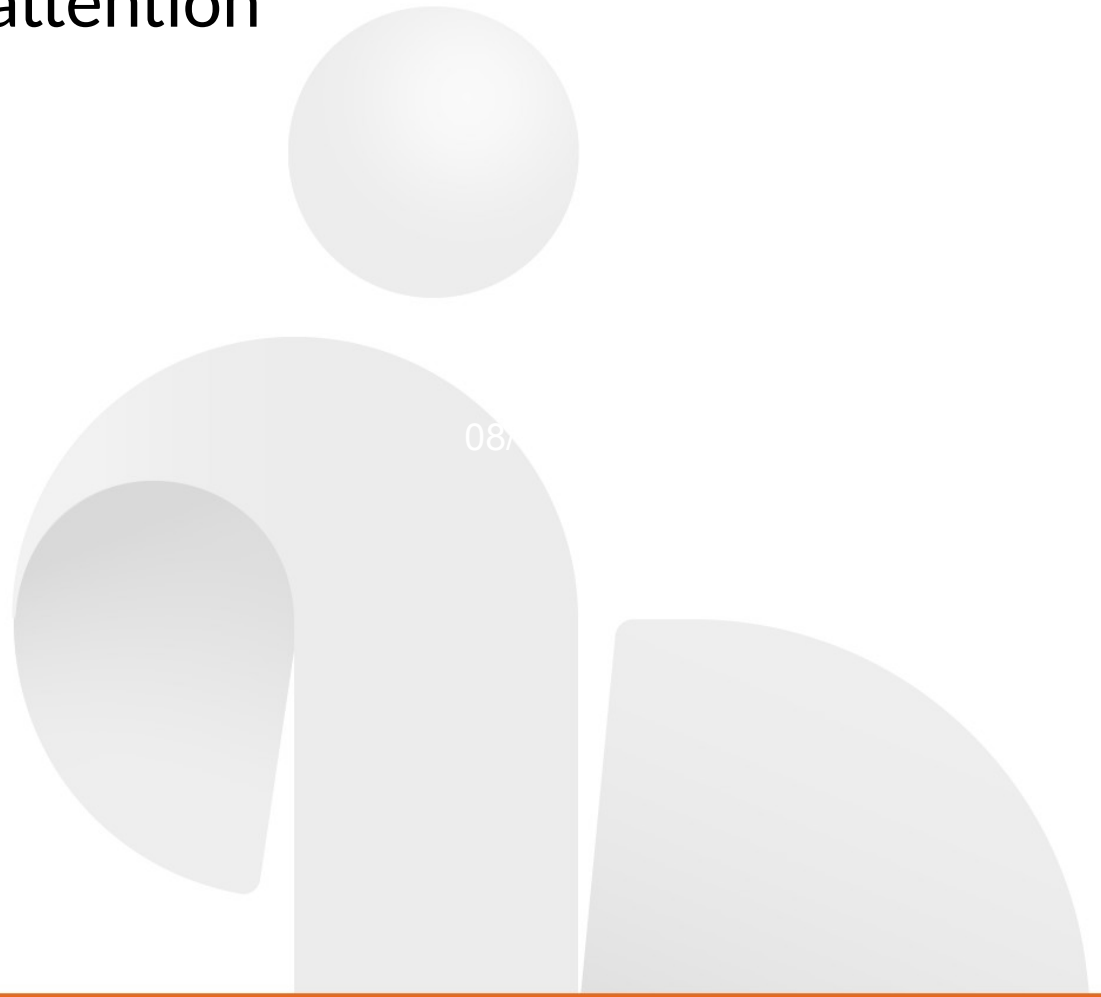


- **Distance influences** > 50km
  - Modification of the fiber polarization
  - Very preliminary development

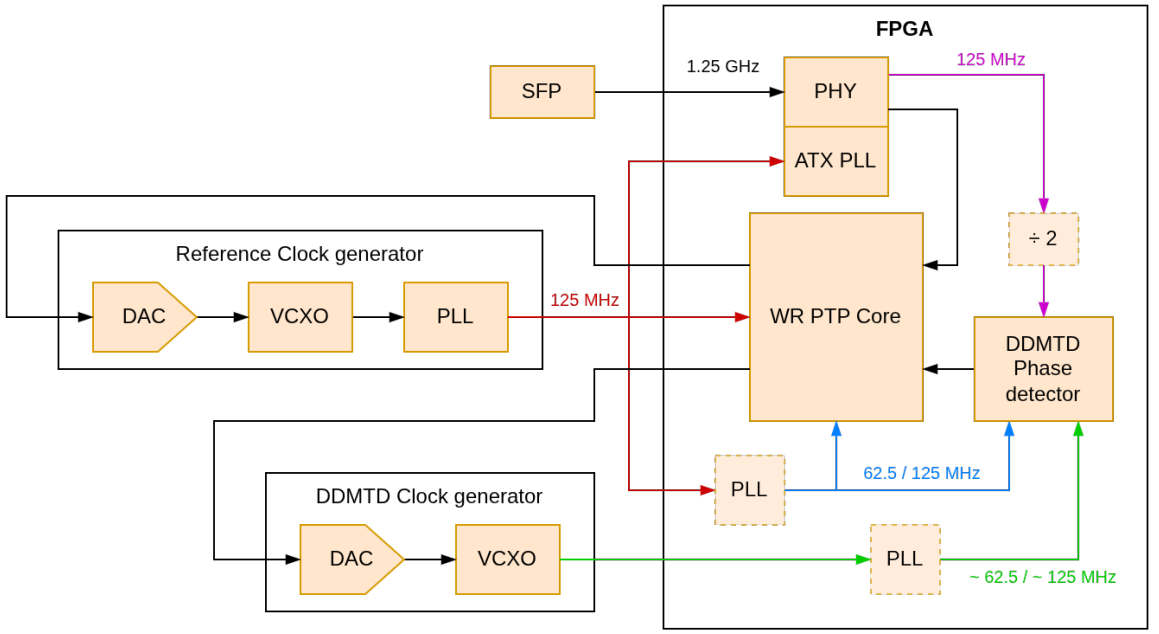
Conclusion

- Very promising results with IDROGEN board (sub-picosecond RMS jitter)
- New board version (v4) with new functionalities and news adding boards
- New projects: CTAO-MST, NENUFAR (Nançay observatory), ATF LLREF, KEK accelerators, New Comet (Nuclear physics @ IJClab), PERLE….
- Focus on essential performances improvements :
    - low-frequency phase noise → WR configuration, software, Firmware
    - Distances → news developments
- White Fox project (jitter < 100fs) for future applications (FCC, Einstein Telescope,…)

Thanks for your attention



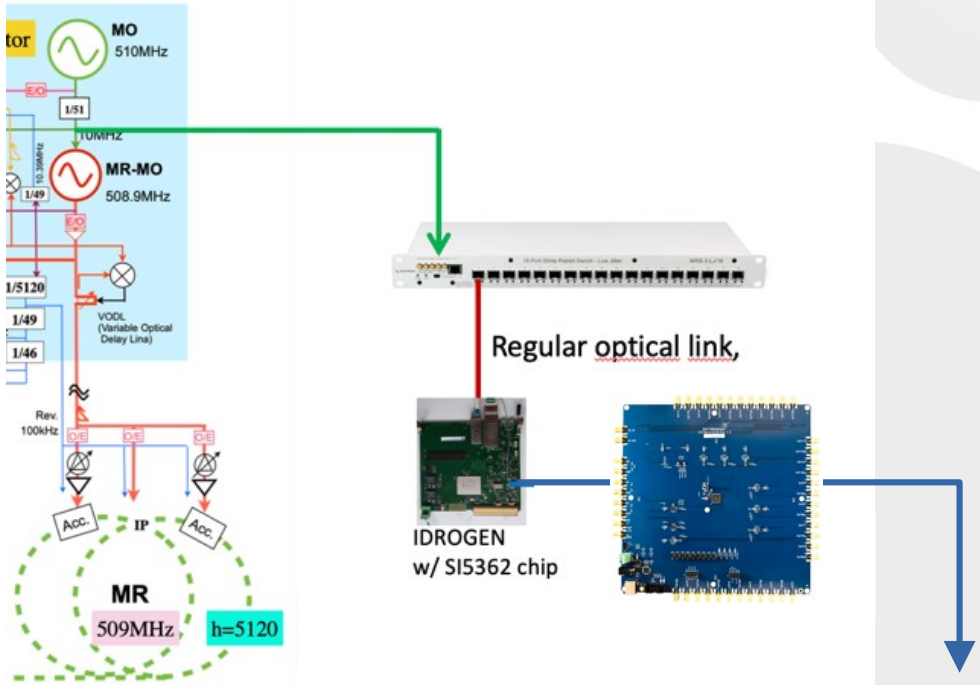
IDROGEN board : WhiteRabbit implementation



- Based on CERN open hardware with Enhancements
- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
  - Tx/Rx routing equalisation

Clock synthesis for accelerators

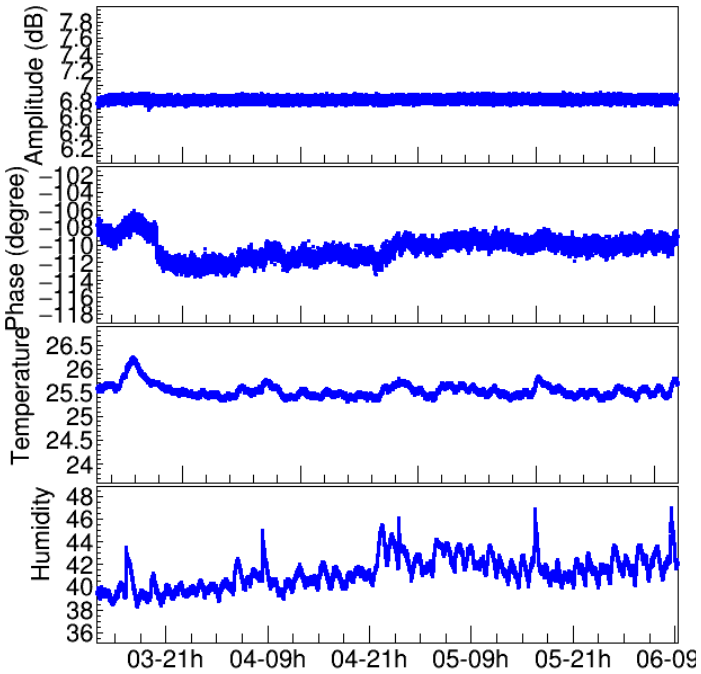
Last result of Super KEK B clock synchronization with IJCLab IDROGEN board.



Comparison of SKB and Idrogen clocks
10h persistency, at scope resolution limit

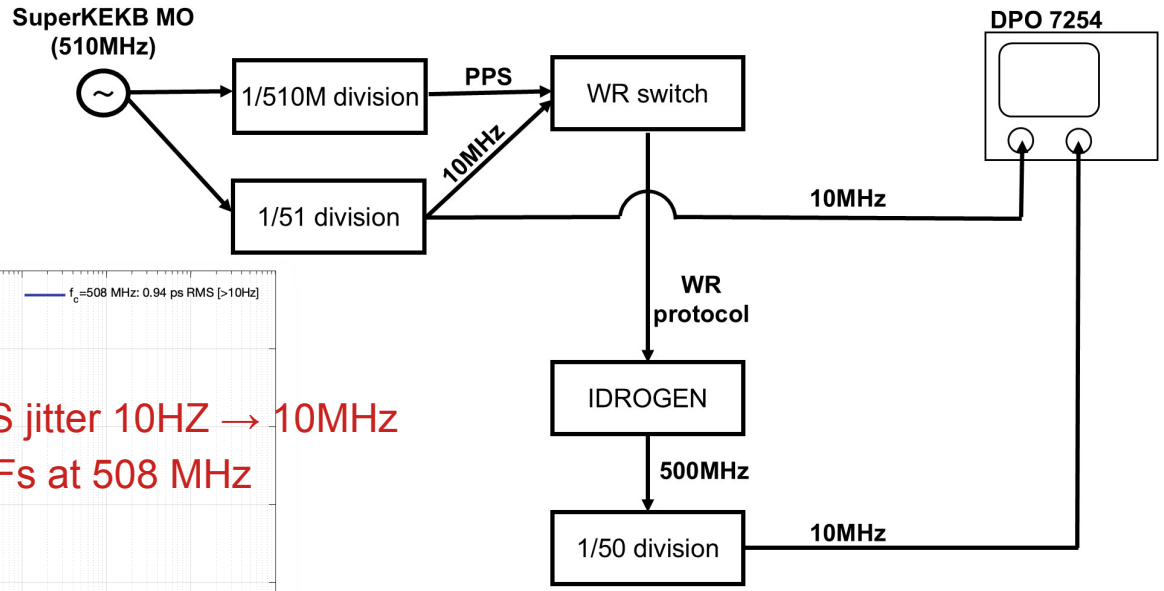


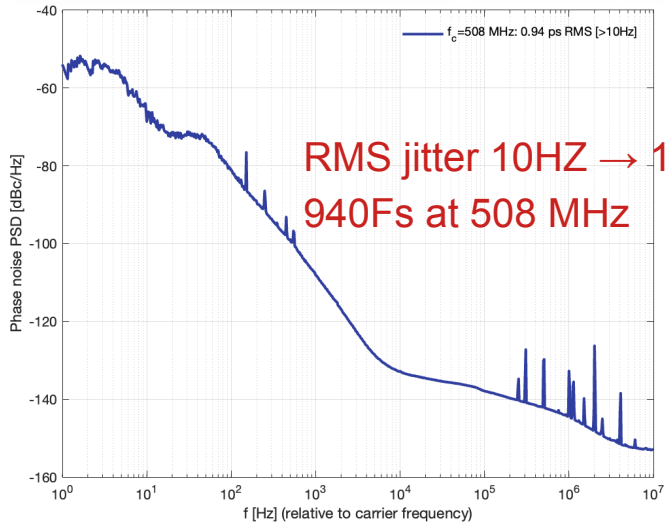
SuperKEKb : Master oscillator distribution



509Mhz

IDROGEN synchronization setup





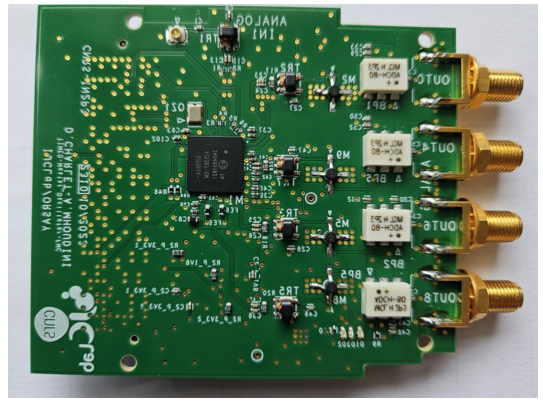
RMS jitter 10HZ → 10MHz
940Fs at 508 MHz

Data taken from Sep22 19:10 to Sep24 12:00

Accelerator synchronization: Arbitrary clock signal synthesizer

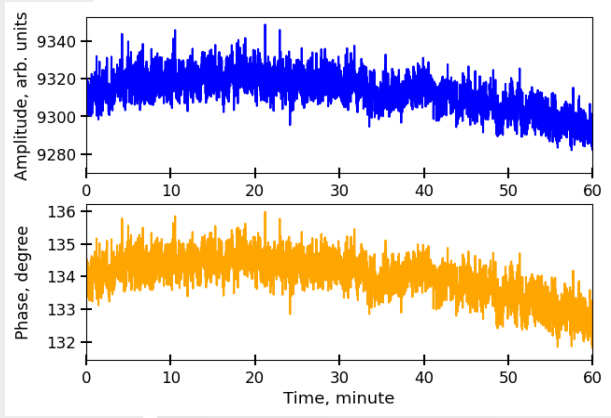
Fractionnal PLL (FPLL) FMC (on test)

- Replace very expensive system with recent, 30€ component
- Generate arbitrary frequency disciplined by WR clock
  - Frequency resolution 1 Hz
  - Phase noise system: 1.7ps (1 Hz, 10 MHz)
  - ~0.3° RMS phase jitter at 375MHz below 1Hz
  - 4 outputs 10KHz to 1.3GHz (2.75GHz: SI5361H chip)

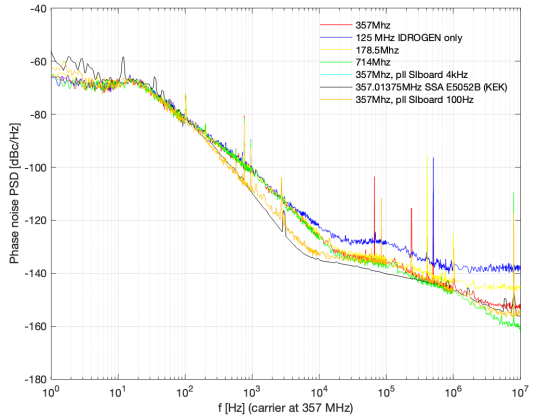


RTM board extension (under test)

- Arbitrary synthesizer
- High performance extension for optical time transfer (White Fox)



Long term drift



Phase noise for various different output frequencies

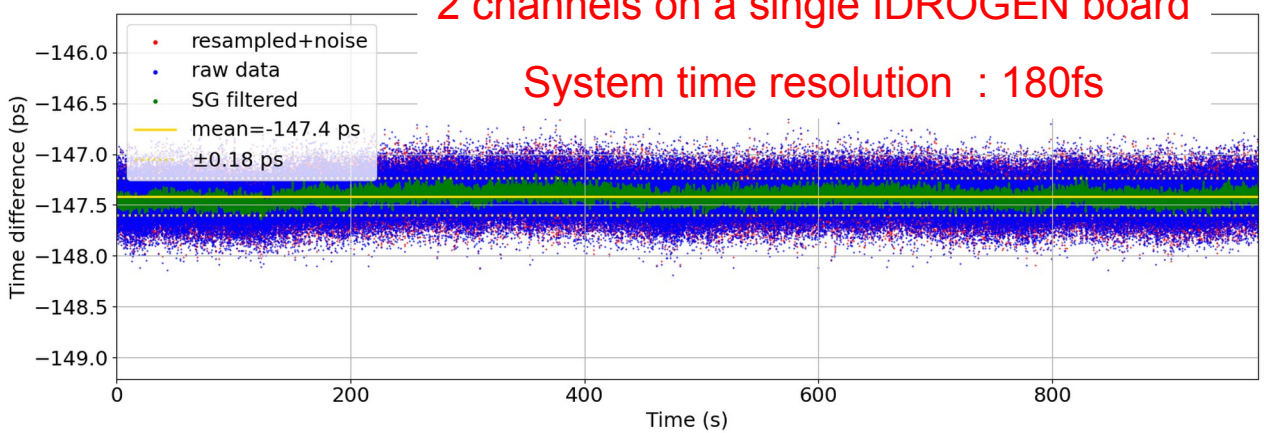
1GSPS ADC board: Synchronization performance

- Bandwidth (single board):
  ~500Mhz (1GHz → 1.5GHz)

- 2 IDROGEN boards synchronized by WR
- 2 channels 1GSPS 14b ADC
- Same RF signal (312.5MHz) split on boards
- FFT 8k point
- Cross correlation

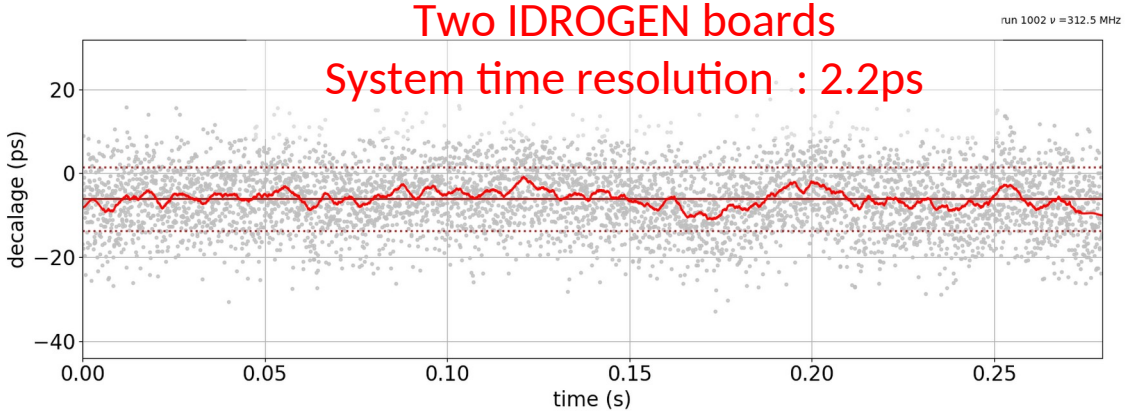
2 channels on a single IDROGEN board

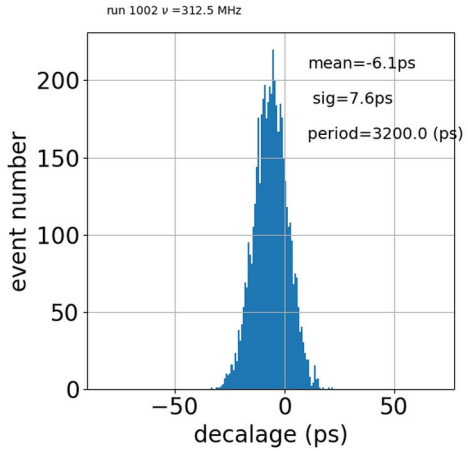
System time resolution : 180fs

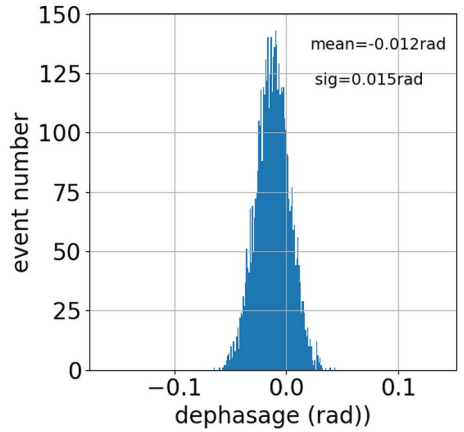


Two IDROGEN boards

System time resolution : 2.2ps



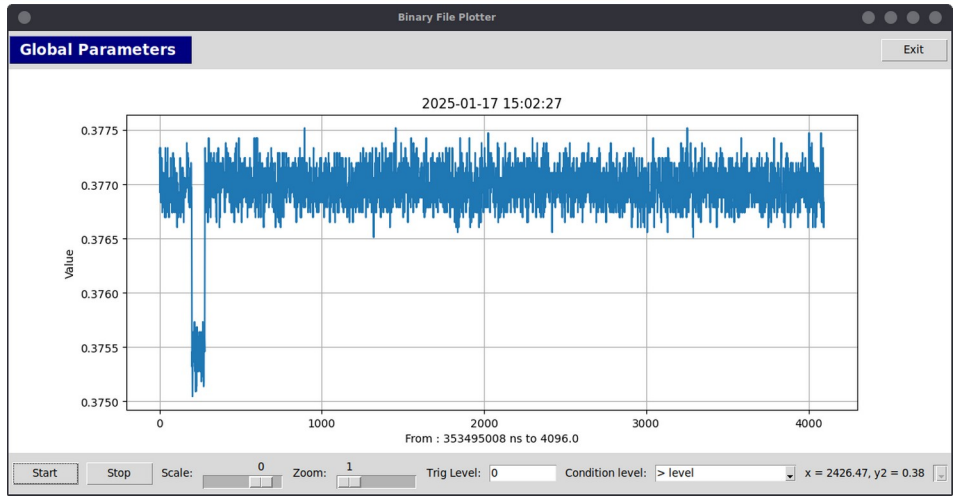


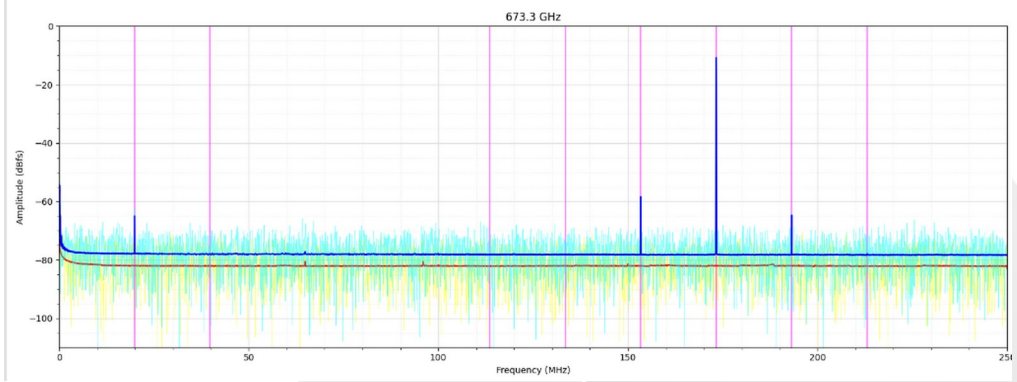


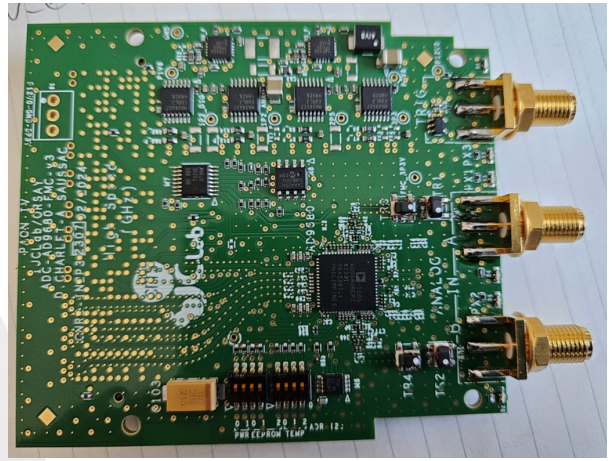
ADC acquisition board

Development of custom ADC board: Using the IDROGEN on board low jitter WhiteRabbit clock

- **FMC ADC9680_V1** (2022)
  - 2 channels, 500 MSPS, 14 bits
  - 2GHz analog bandwidth
  - Clock provided by Idrogen board
- **FMC ADC9680_V3** (2024)
  - 2 channels, 1 GSPS, 14 bits
- **FMC ADS42JB69** (2025)
  - 4 channels, 250 MSPS, 16bits
  - One external trigger
  - Analog input 900MHz
  - 2.5V inputs voltage







IJClab setup

